# 1. Introduction

Even though triacs have been available since the 1960s and are regarded as a mature technology, they remain an extremely popular power control device for AC mains applications because of their low cost and the simplicity of their control circuits. There was even an upsurge in their use from the 1990s due partly to the increased use of domestic appliances with electronic controls. Common examples of these appliances include air and water heaters, vacuum cleaners, refrigerators, washing machines, dishwashers, coffee machines, air conditioning units and most small kitchen appliances.

Despite its maturity, triac technology has not "stood still" since the invention of the first triacs. Triacs have evolved to meet the changing demands of applications. One such important change is the gate sensitivity specification, $I_{GT}$. Early triac trigger circuits were built using discrete components that could supply substantial currents of 100mA peak or more. These are still relevant today for discrete phase control circuits which use a diac to deliver healthy, well-defined trigger pulses. However, for two main reasons, Integrated Circuit control has become increasingly popular and this required more sensitive gates driven by smaller gate currents.

Firstly, Electro Magnetic Compatibility regulations limit the harmonic currents that can be drawn from the mains and also limit the amount of Radio Frequency Interference that can be generated by appliances. This requires the use of a dedicated zero crossing triac power control IC or, more likely nowadays, a microcontroller with suitable programming to achieve the required functions. One example is where a high harmonic and RFI-generating phase control circuit is replaced by an electrically "quieter" alternative that is suitable for variable power control of higher power or resistive loads. An example of this is a Binary Rate Modulation power controller in which varying full and half mains cycles are conducted symmetrically to ensure very low harmonic currents and zero DC component in the current waveform.

Secondly, more intelligent appliance controls have become common place, such as remote control, soft start, variable timing, automatic power ramp-up & ramp-down and intelligent power control. These would be very complicated, expensive or even impossible to implement using discrete components. Integrated Circuits (microcontrollers) must be used, but they possess a limited drive current capability of 10 or 20mA max. Furthermore, since the IC's supply is sometimes derived from the mains via a basic resistive/capacitive dropper and half-wave rectifier, current availability is limited and the average current demand from the IC's power supply must be minimised. This imposes a limit on the current amplitude and duration available for triggering the triac.

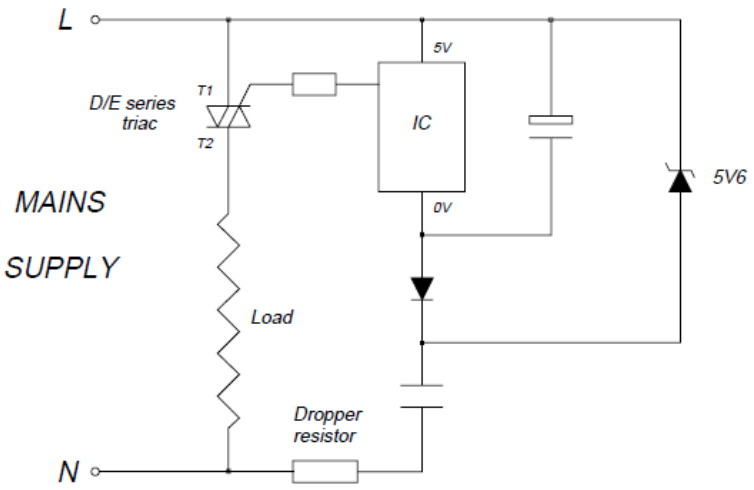



Fig. 1 A typical IC / Triac circuit arrangement

Fig. 1 shows a simple *low-cost* IC-triac arrangement. The 5.6V Zener diode combined with the forward voltage drop of the rectifier diode produce an IC supply close to 5V. The advantages of connecting the Zener as shown instead of directly across the IC are that full wave current is drawn from the mains supply (no DC component), and the forward conduction of the Zener means that the diode never has to support full mains voltage. A cheap, low voltage diode can therefore be used. Attention must be paid, however, to the additional power dissipation in the resistor due to the forward Zener current.

These IC-triac power control applications could not be implemented without sensitive gate triacs. WeEn logic level D series and sensitive gate E series triacs are designed to meet fully the requirements in this established market. For a full selection guide of available types, see Tables 1 and 2 on pages 8, 9 and 10.

## 2. Gate trigger current, $I_{GT}$

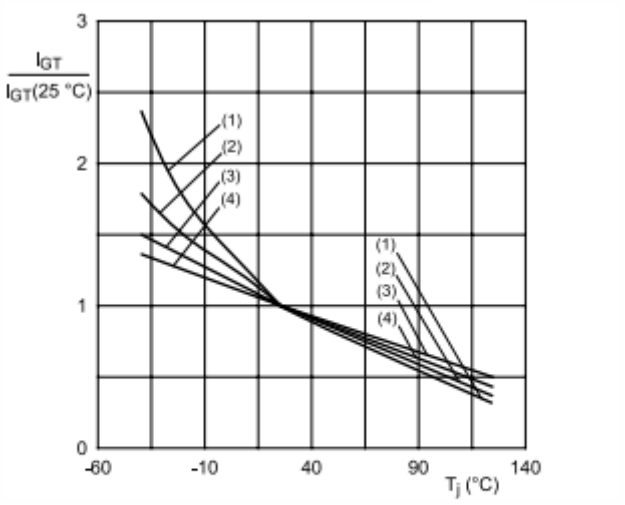
WeEn's D and E series of the older designed four-quadrant (4Q) triacs are specified to trigger in all four triggering quadrants. 4Q triacs have the unavoidable limitation of being less sensitive and more difficult to trigger in the 4th (T2-, G+) quadrant. (For example, for the D series, max $I_{GT}$ in quadrant 1, 2, 3 and 4 is 5, 5, 5 and 10mA, and for the E series it is 10, 10, 10 and 25mA). In the 4th quadrant, the ability of triacs to support a high rate of rise of load current ($dI_T$ /dt) after turn-on is also limited as $dI_T/dt$ can be 10A/µs compared with 50A/µs or higher in the other three quadrants.

For these two reasons, operation in the 4th quadrant is not recommended and is best avoided. Consequently, WeEn developed a range of three quadrant (3Q) triacs specified to trigger in only 3 quadrants with a specification for $dI_T/dt$ = 100A/µs in all three quadrants. These are the 3Q Hi-Com triac series with vastly superior immunity to commutation failure / loss of control compared to the more traditional 4Q alternatives. Three-quadrant triacs are the automatic first choice for any application. (For triggering quadrant diagram refer to the Appendix on page 11)

Since the control IC operates on a single rail supply (usually +5V), its outputs are unipolar and therefore can be referenced to the mains circuit in order to source current (positive gate drive) or to

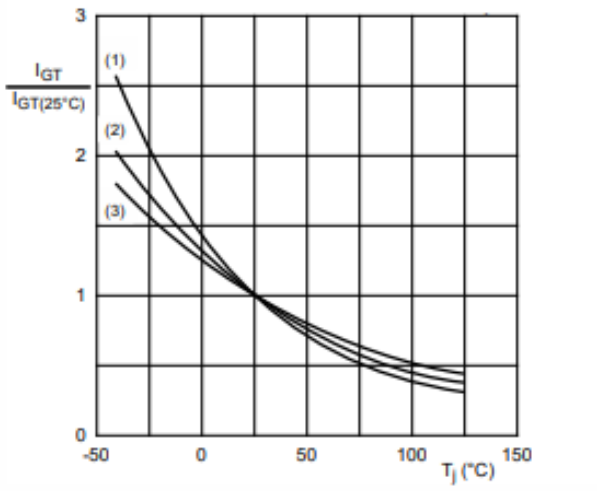
sink current (negative gate drive). Since 4th quadrant triggering should be avoided, the optimum performance will be obtained with negative gate current - i.e. operation in the 2nd (T2+, G-) and 3rd (T2-, G-) triggering quadrants (see Fig. 1).

A triac's $I_{GT}$ increases at lower temperatures and the gate drive circuit must supply enough gate current for the lowest expected operating temperature to guarantee triggering. Fig. 2 shows an example of normalised $I_{GT}$ versus $T_j$ for the 4Q BT136 series D and Fig. 3 for the 3Q BTA310-600D.




(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

Fig. 2 BT136 series D normalised $I_{GT}$ versus $T_j$




(1) T2- G-
(2) T2+ G-
(3) T2+ G+

Fig. 3 BTA310 series D normalised $I_{GT}$ versus $T_j$

# 3. Latching current, $I_L$

If the triac is triggered by a gate current at the beginning of a mains half-cycle, the load current will build up gradually from zero. The gate current must not be removed before the triac is latched ON otherwise it will return to the blocking state. Latching occurs when the load current reaches $I_L$. The gate pulse must therefore be present until the load current has reached $I_L$.

Just as for $I_{GT}$, the holding current, $I_L$ also increases at lower temperature. The gate pulse duration must be specified at the lowest expected operating temperature for guaranteed triggering. Fig. 4 shows an example of normalised $I_L$ versus $T_j$ for the 4Q BT136 series D and Fig. 5 for the 3Q BTA310 series D.

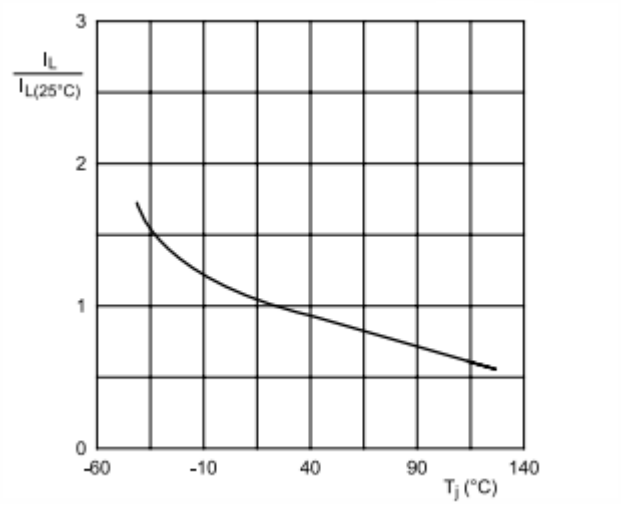



Fig. 4 BT136 series D normalised $I_L$ versus $T_j$

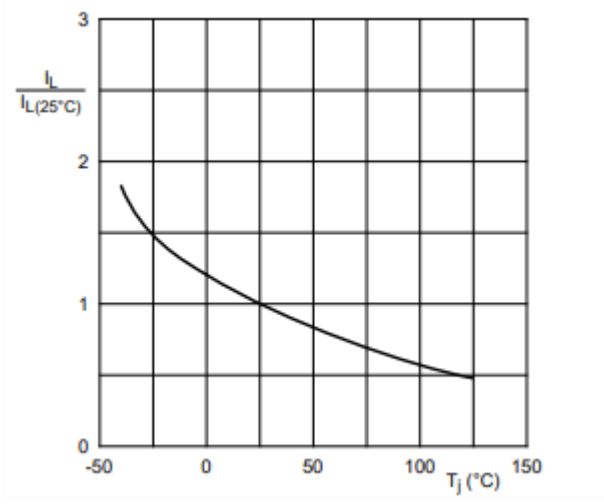



Fig. 5 BTA310 series D normalised $I_L$ versus $T_j$

How quickly the load current reaches the triac's latching current, $I_L$ will depend on the peak load current and mains frequency. Taken to the extreme case, if the load current is so low that its peak value is equivalent to $I_L$, it will take one quarter cycle, or 5ms for 50Hz mains, before the triac is latched and the gate pulse can cease.

It is also important to be aware that higher current triacs have a higher latching current, $I_L$. This could increase switching problems or even lead to the triac never latching ON if the load current is lower than the triac's $I_L$. So, apart from the higher component cost, it would not be advisable to use a triac whose current rating is very much higher than the load current when a lower current type is available. Tables 1 and 2 on pages 8, 9 and 10, illustrate how $I_L$ varies with the triggering quadrant and triac current rating.

# 4. Calculating the minimum average triac current

Because the current demand must be minimised in many IC applications, it is necessary to calculate the gate pulse duration to be just long enough to guarantee triac triggering while avoiding unnecessary burden on the IC's power supply. The time to reach $I_L$, hence the gate pulse duration, can be calculated using the equation:

$$\mathbf{I_L = I_{pk} \times \sin(2\pi ft)}$$

Transposing gives:

$$\mathbf{t = 1/(2\pi f) \times \sin^{-1}(I_L/I_{pk})}$$

The average gate current supplied by the IC is calculated by multiplying its peak gate current with t/T.

Hence:

$$\mathbf{I_{G(av)} = I_{G(pk)} \times t/T}$$

$\mathbf{I_L}$ = triac latching current at the lowest expected operating-temperature

$\mathbf{I_{pk}}$ = peak load current

**t** = gate pulse duration

**T** = gate pulse cycle time.

Note:- Since triac latching current is higher in the 2nd and 4th quadrants, and normal operation for IC triggering is in the 2nd and 3rd quadrants, the gate current calculations must always be based on *the worst-case quadrant 2, $I_L$ condition.*

If the load current is very low and the necessary gate pulse duration imposes too great a burden on the IC's power supply, triggering could be delayed for a few degrees to allow the supply voltage to build up a little. The time to reach $I_L$ will then be shortened by the delay time (true for resistive loads). Now that switching occurs further from the zero crossing, there will be a slightly increased risk of RFI generation, even if the load current is very low as in this case. RFI measurements will show if filtering is necessary to meet the relevant EMC regulations.

# 5. Holding current, $I_H$

As the load current reduces towards the end of a mains half cycle, a current, $I_H$, will be reached when the triac is no longer latched. It will cease to conduct in the absence of a gate current. $I_H$ also increases with reducing temperature. Fig. 6 shows an example of normalised $I_H$ versus $T_j$ for the 4Q BT136 series D and Fig. 7 for the 3Q BTA310 series D.

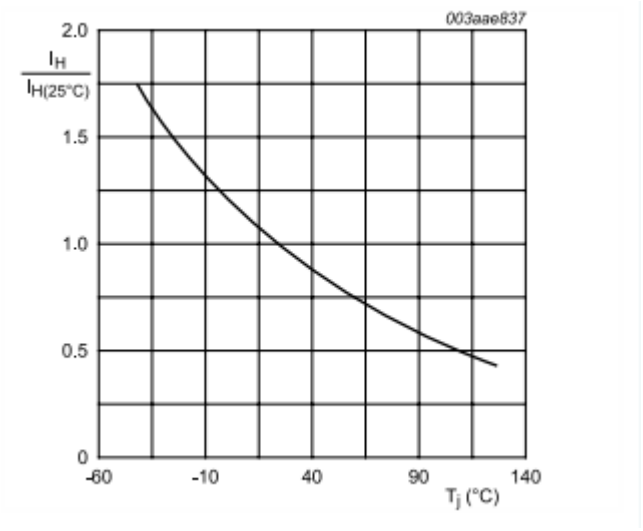



Fig. 6 BT136 series D normalised $I_H$ versus $T_j$

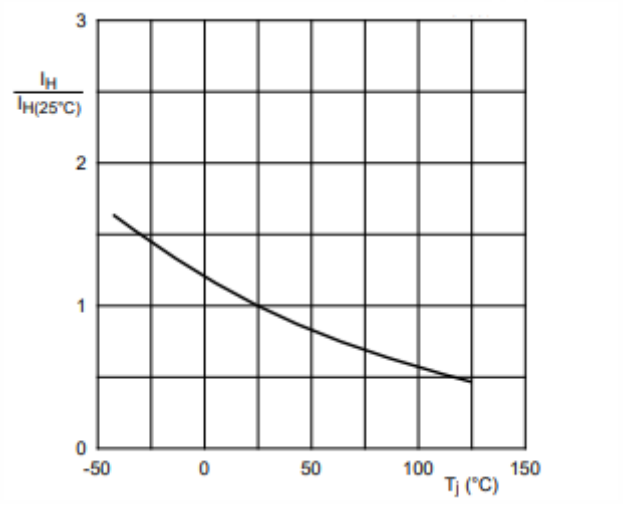
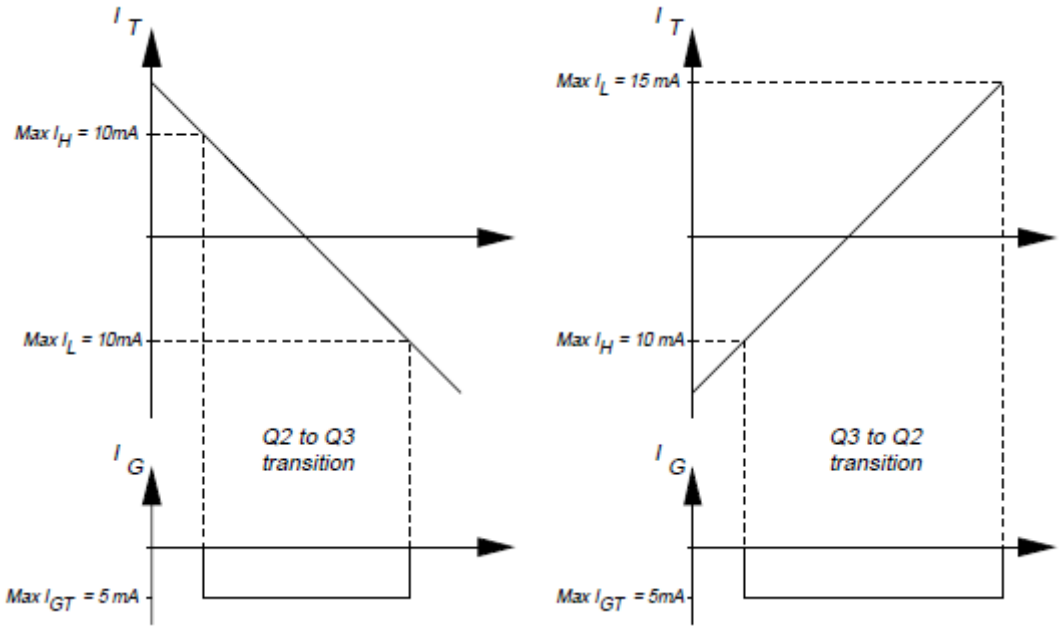



Fig. 7 BTA310 series D normalised $I_H$ versus $T_j$

In some IC applications where the triac is used as a power switch, for example a precision electronic thermostat for a refrigerator compressor, continuous conduction must be maintained through the current zero crossing. (This is essential to prevent glitches and RFI generation). Continuous conduction is achieved by monitoring the load current and applying a gate pulse before the triac's $I_H$ is reached and maintaining the pulse until the current has passed through zero and risen to the triac's $I_L$ in the alternate quadrant. This condition must be met at the lowest expected operating temperature for continuous glitch-free conduction under worst-case conditions.

The holding current, $I_H$ increases for the larger E series triacs whereas the most sensitive D series triacs are designed to maintain a consistent, low $I_H$ of 10mA @ 25˚C even for the higher current rating.

Fig. 8 illustrates triac load current zero-crossing and the minimum gate pulse required for continuous conduction through the max $I_H$ and $I_L$ points. The diagram illustrates how $I_H$ remains constant in different quadrants. The point made earlier about how $I_L$ varies in different quadrants is illustrated by the higher $I_L$ in the 2nd quadrant (T2+, G-). Note that the $I_G$ duration must meet this worst-case condition.



# Logic level selection guide (at June 2020)

**Table 1. 3Q Logic level and sensitive gate triacs**

| Triac Type Number | Gate Sensitivity | $I_{T(RMS)}$ (A) | $V_{DRM}$ (V) | $I_{GT(max)}$ (mA) | $I_{L(max)}$ (mA) | $I_{H(max)}$ (mA) | Package |
|---|---|---|---|---|---|---|---|
| BTA2008W | D | 0.8 | 600D & 800D | 5 | 20 | 10 | SOT223 |
| BTA2008 | D/E | 0.8 | 600D/E & 800D | 5/10 | 12/20 | 12 | TO92 |
| BTA2008 | D | 0.8 | 1000D | 5 | 20 | 10 | TO92 |
| BTA201 | E | 1 | 600E & 800E | 10 | 20 | 12 | TO92 |
| BTA201W | E | 1 | 600E & 800E | 10 | 12 | 12 | SOT223 |
| BTA202X | D/E | 2 | 600D/E & 800D/E | 5/10 | 5/20 | 10/12 | TO220F |
| BTA204 | D/E | 4 | 600D/E & 800E | 5/10 | 9/18 | 6/12 | TO220AB |
| BTA204S | D/E | 4 | 600D/E & 800E | 5/10 | 9/18 | 6/12 | DPAK |
| BTA204W | D/E | 4 | 600D/E & 800E | 5/10 | 9/18 | 6/12 | SOT223 |
| BTA204X | D/E | 4 | 600D/E & 800E | 5/10 | 9/18 | 6/12 | TO220F |
| BTA206 | E | 6 | 800E | 10 | 30 | 15 | TO220AB |
| BTA206X | E | 6 | 800E | 10 | 30 | 15 | TO220F |
| BTA208 | D/E | 8 | 600D/E & 800E | 5/10 | 25/18 | 15/12 | TO220AB |
| BTA208S | D/E | 8 | 600D/E & 800E | 5/10 | 25/30 | 15/25 | DPAK |
| BTA208X | D/E | 8 | 600D/E & 800E | 5/10 | 9/18 | 6/12 | TO220F |
| BTA310 | D/E | 10 | 600D/E & 800D/E | 5/10 | 15/30 | 10/15 | TO220AB |
| BTA310X | D/E | 10 | 600D/E & 800D/E | 5/10 | 15/30 | 10/15 | TO220F |
| BTA410 | E | 10 | 600E & 800E | 10 | 30 | 15 | TO220AB |
| BTA410X | E | 10 | 600E & 800E | 10 | 30 | 15 | TO220F |
| BTA410Y | E | 10 | 600E & 800E | 10 | 30 | 15 | IITO220 |
| BTA312 | D/E | 12 | 600D/E & 800E | 5/10 | 15/30 | 10/15 | TO220AB |
| BTA312X | D/E | 12 | 600D/E & 800E | 5/10 | 15/30 | 10/15 | TO220F |
| BTA312B | D/E | 12 | 600D/E & 800E | 5/10 | 15/30 | 10/15 | $D^2PAK$ |
| BTA412Y | E | 12 | 600E & 800E | 10 | 35 | 10 | IITO220 |
| BTA316 | D/E | 16 | 600D/E & 800E | 5/10 | 30/30 | 15/15 | TO220AB |
| BTA316X | E | 16 | 600E & 800E | 10 | 30 | 25 | TO220F |
| BTA316B | E | 16 | 600E & 800E | 10 | 30 | 15 | $D^2PAK$ |

Fig. 8 Example of relationship between $I_L$, $I_H$ and $I_{GT}$ (for BT136 series D at 25°C)

**Table 2. 4Q Logic level and sensitive gate triacs**

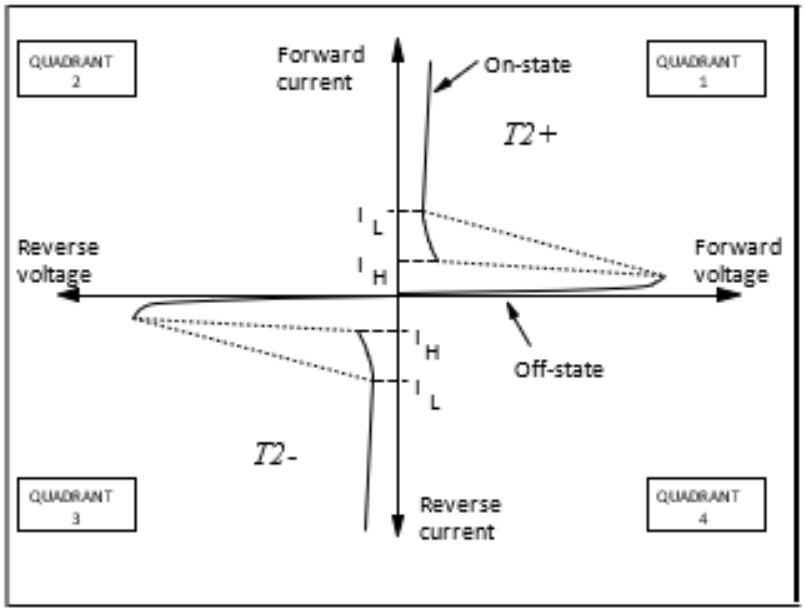
| Triac Type Number | Gate Sensitivity | $I_{T(RMS)}$ (A) | $V_{DRM}$ (V) | $I_{GT(max)}$ (mA) | $I_{L(max)}$ (mA) | $I_{H(max)}$ (mA) | Package |
|---|---|---|---|---|---|---|---|
| MAC97A6 | very sensitive | 0.6 | 400 | 5,5,5,7 | 10 | 10 | TO92 |
| MAC97A8 | very sensitive | 0.8 | 600 | 5,5,5,7 | 10 | 10 | TO92 |
| BT131W | very sensitive | 1 | 600 | 3,3,3,7 | 8 | 5 | SOT223 |
| BT131 | very sensitive | 1 | 600 & 800 | 3,3,3,7 | 8 | 5 | TO92 |
| BTA131 | D/E | 1 | 600D/E & 800D/E | 5,5,5,7/10 | 20/25 | 10/10 | TO92 |
| Z0103MA | very sensitive | 1 | 600 | 3,3,3,5 | 15 | 7 | TO92 |
| ZO103NA | very sensitive | 1 | 800 | 3,3,3,5 | 15 | 7 | TO92 |
| Z0103MN | very sensitive | 1 | 600 | 3,3,3,5 | 15 | 7 | SOT223 |
| ZO103NN | very sensitive | 1 | 800 | 3,3,3,5 | 15 | 7 | SOT223 |
| Z0107MA | very sensitive | 1 | 600 | 5,5,5,7 | 20 | 10 | TO92 |
| Z0107NA | very sensitive | 1 | 800 | 5,5,5,7 | 20 | 10 | TO92 |
| Z0107MN | very sensitive | 1 | 600 | 5,5,5,7 | 20 | 10 | SOT223 |
| Z0107NN | very sensitive | 1 | 800 | 5,5,5,7 | 20 | 20 | SOT223 |
| Z0109MA | sensitive | 1 | 600 | 10 | 25 | 10 | TO92 |
| Z0109NN | sensitive | 1 | 800 | 10 | 25 | 20 | TO92 |
| Z0109MN | sensitive | 1 | 600 | 10 | 25 | 10 | SOT223 |
| Z0109NN | sensitive | 1 | 800 | 10 | 25 | 10 | SOT223 |
| Z0103MA0 | sensitive | 1 | 600 | 3,3,3,5 | 20 | 7 | TO92 |
| ZO103NA0 | sensitive | 1 | 800 | 3,3,3,5 | 20 | 7 | TO92 |
| Z0103MN0 | sensitive | 1 | 600 | 3,3,3,5 | 20 | 7 | SOT223 |
| ZO103NN0 | sensitive | 1 | 800 | 3,3,3,5 | 20 | 7 | SOT223 |
| Z0107MA0 | sensitive | 1 | 600 | 5,5,5,7 | 25 | 10 | TO92 |
| Z0107NA0 | sensitive | 1 | 800 | 5,5,5,7 | 25 | 10 | TO92 |
| Z0107MN0 | sensitive | 1 | 600 | 5,5,5,7 | 25 | 10 | SOT223 |
| Z0107NN0 | sensitive | 1 | 800 | 5,5,5,7 | 25 | 10 | SOT223 |
| Z0109MA0 | sensitive | 1 | 600 | 10 | 30 | 10 | TO92 |
| Z0109NA0 | sensitive | 1 | 800 | 10 | 30 | 10 | TO92 |
| Z0109MN0 | sensitive | 1 | 600 | 10 | 30 | 10 | SOT223 |
| Z0109NN0 | sensitive | 1 | 800 | 10 | 30 | 10 | SOT223 |
| BT132 | D | 1 | 600 | 5,5,5,10 | 15 | 10 | TO92 |
| BT134W | D | 1 | 600D | 5,5,5,10 | 15 | 10 | SOT223 |
| BT134W | E | 1 | 600E & 800E | 10,10,10,25 | 20 | 15 | SOT223 |
| BT134 | D | 4 | 600D | 5,5,5,10 | 15 | 10 | SOT82 |
| BT134 | E | 4 | 600E & 800E | 10,10,10,25 | 20 | 15 | SOT82 |
| BT136 | D | 4 | 600D | 5,5,5,10 | 15 | 10 | TO220AB |
| BT136X | D | 4 | 600D | 5,5,5,10 | 15 | 10 | TO220F |
| BT136S | D | 4 | 600D | 5,5,5,10 | 15 | 10 | DPAK |
| BT136 | E | 4 | 600E & 800E | 10,10,10,25 | 20 | 15 | TO220AB |
| BT136X | E | 4 | 600E & 800E | 10,10,10,25 | 20 | 15 | TO220F |
| BT136S | E | 4 | 600E & 800E | 10,10,10,25 | 20 | 15 | DPAK |
| BT136B | E | 4 | 600E & 800E | 10,10,10,25 | 20 | 15 | $D^2PAK$ |

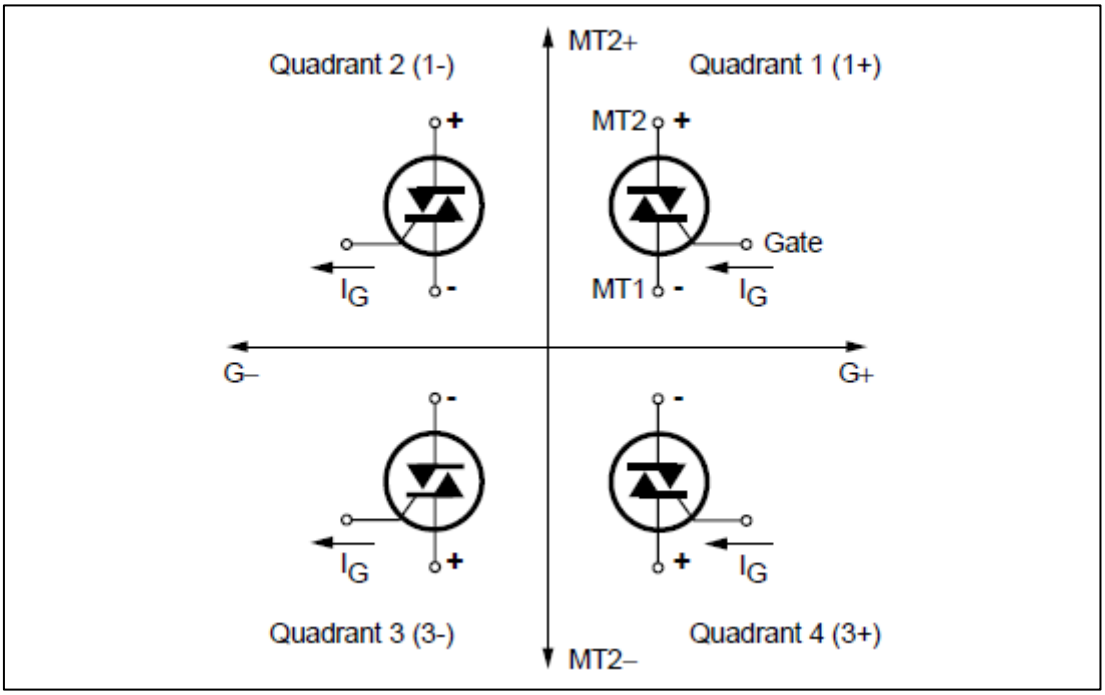
**Table 2. 4Q Logic level and sensitive gate triacs**
**(continued)**

| Triac Type Number | Gate Sensitivity | $I_{T(RMS)}$ (A) | $V_{DRM}$ (V) | $I_{GT(max)}$ (mA) | $I_{L(max)}$ (mA) | $I_{H(max)}$ (mA) | Package |
|---|---|---|---|---|---|---|---|
| BT234 | D | 4 | 600D & 800D | 5,5,5,10 | 15 | 6 | TO220AB |
| BT234 | E | 4 | 600E & 800E | 10,10,10,25 | 25 | 15 | TO220AB |
| BT234X | D | 4 | 600D & 800D | 5,5,5,10 | 15 | 6 | TO220F |
| BT234X | E | 4 | 600E & 800E | 10,10,10,25 | 25 | 15 | TO220F |
| BT137 | D | 8 | 600D | 5,5,5,10 | 20 | 10 | TO220AB |
| BT137 | E | 8 | 600E & 800E | 10,10,10,25 | 35 | 20 | TO220AB |
| BT137X | D | 8 | 600D | 5,5,5,10 | 20 | 10 | TO220F |
| BT137X | E | 8 | 600E & 800E | 10,10,10,25 | 35 | 20 | TO220F |
| BT137S | D | 8 | 600D | 5,5,5,10 | 20 | 10 | DPAK |
| BT137S | E | 8 | 600E & 800E | 10,10,10,25 | 35 | 20 | DPAK |
| BT137B | E | 8 | 600E | 10,10,10,25 | 35 | 20 | $D^2PAK$ |
| BT138 | D | 12 | 600D | 5,5,5,10 | 20 | 10 | TO220AB |
| BT138 | E | 12 | 600E & 800E | 10,10,10,25 | 40 | 30 | TO220AB |
| BT138X | D | 12 | 600D | 5,5,5,10 | 20 | 10 | TO220F |
| BT138X | E | 12 | 600E & 800E | 10,10,10,25 | 40 | 30 | TO220F |
| BT138B | E | 12 | 600E & 800E | 10,10,10,25 | 40 | 30 | $D^2PAK$ |
| BT138Y | E | 12 | 600E & 800E | 10,10,10,25 | 40 | 30 | IITO220AB |
| BT139 | E | 16 | 600E & 800E | 10,10,10,25 | 40 | 45 | TO220AB |
| BT139X | E | 16 | 600E | 10,10,10,25 | 40 | 45 | TO220F |
| BT139B | E | 16 | 600E & 800E | 10,10,10,25 | 40 | 45 | $D^2PAK$ |

# 7. Appendix

**1. Triac V/I characteristics and triggering quadrants**




**2. WeEn Semiconductors Product Selection Guide:-**

http://www.ween-semi.com/sites/default/files/inline-files/WeEn20190626.pdf

## Revision history

| Rev | Date | Description |
|---|---|---|
| v.01 | 20200701 | New Application Note |
| v.02 | 20200716 | Addition to 1st paragraph on page 7 |

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