1. Introduction

There is an ever-growing need in the electronics industry for miniaturization and cost reduction. To satisfy these requirements, designers are specifying Surface-Mount Technology (SMT) increasingly. Their attentions were firstly aimed at the low power and small signal components and afterwards their attentions were turned towards power devices to give total surface-mount solutions.

The increased miniaturization is possible because surface mounted power semiconductors occupy less board area than through-hole-mounted devices on heatsinks. Cost reduction is possible due to the faster and simpler assembly that result when ALL components are surface mounted.

The availability of a wide range of package sizes permits continuous power dissipations ranging from 0.5W to 2W on standard Printed-Circuit Boards (PCB). Higher power dissipations are achievable if special heatsink provisions are made on the PCB. Some examples of these include:

- A grid of solder vias to a pad on the reverse side of the PCB
- A PCB-mounted heatsink on one or both sides
- An aluminium-cored PCB
- Fan-assisted cooling

2. Surface mount packages from WeEn Semiconductors

WeEn Semiconductors has developed a full range of surface-mount power packages for its entire product portfolio. The assembly materials and technology used are not simply adapted from the pre-existing through-hole-mounting package technology; they are unique to SMT.
Every new SMT device is subjected to rigorous testing which originates from stringent automotive requirements. This consists of full reliability testing after three surface mounting operations on printed circuit boards. No failures will be generated. This gives the best assurance of reliable manufactured products.

This technical publication presents the surface-mount packages and shows what thermal performances can be achieved on standard PCBs without special heatsinking arrangements.

3. SOT223

SOT223 (Fig. 1), also known by its JEDEC name TO261, is a commonly used SMT plastic power package of 3 leads with a tab for increased heatsinking. Its mechanical design has been optimized for maximum ease and versatility for surface mounting and maximum long-term reliability in the application. It will provide the minimum cost of ownership to the Original Equipment Manufacturer when initial purchase costs, handling costs and final assembly costs are added together.

The three legs and the heatsink tab emerge sideways from the edge of the plastic body, where they are formed to bring them into contact with the PCB for soldering to the pads. The centre leg and the larger heatsink tab on the opposite side of the package are internally connected.

The main tab and the three legs emerge from the edge of the plastic package and are formed before they contact the PCB. This allows a certain degree of safe PCB movement relative to the device as the assembly expands and contracts during soldering and during circuit operation.

Since the device's die pad is not in direct contact with the PCB solder pad, differential movement caused by different coefficients of expansion can be accommodated without excessive fatigue stress to the solder joints. The more extreme condition of stresses being transmitted to the die, causing it to crack, is also minimized with this package design.

3.1 SOT223 soldering

When soldering most SMT power packages, a reflow process must be used. However, for SOT223, it is also feasible to use wave soldering if required. Wave soldering is possible because the small size of the package minimizes the size of the "shadow" on the downstream side of the solder flow. Perhaps more importantly, the exposed nature of the solder connections around the periphery of the package, and their relatively low thermal capacities, mean that full solder wetting is easily possible with wave soldering. The good visibility of the solder joints allows full inspection for quality after assembly. Fig. 2 and Fig. 3 show the recommended SOT223 footprints for reflow soldering and for wave soldering.

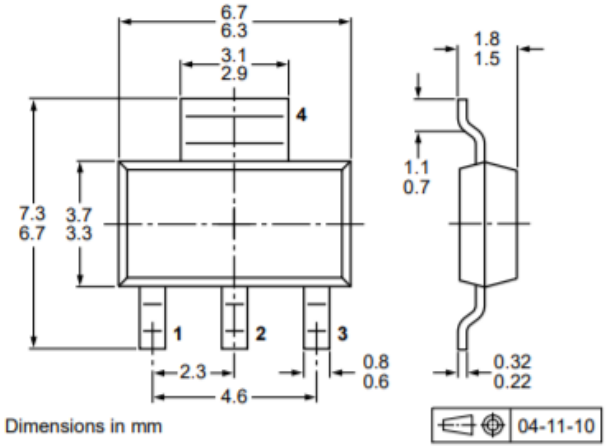


Fig.1 Package outline for SOT223

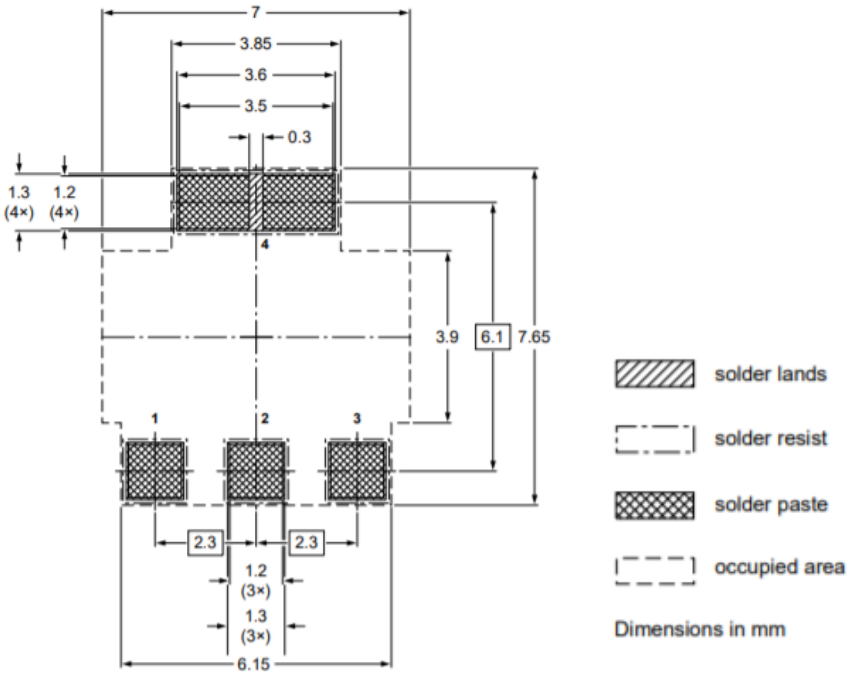


Fig. 2 SOT223 pad layout for reflow soldering

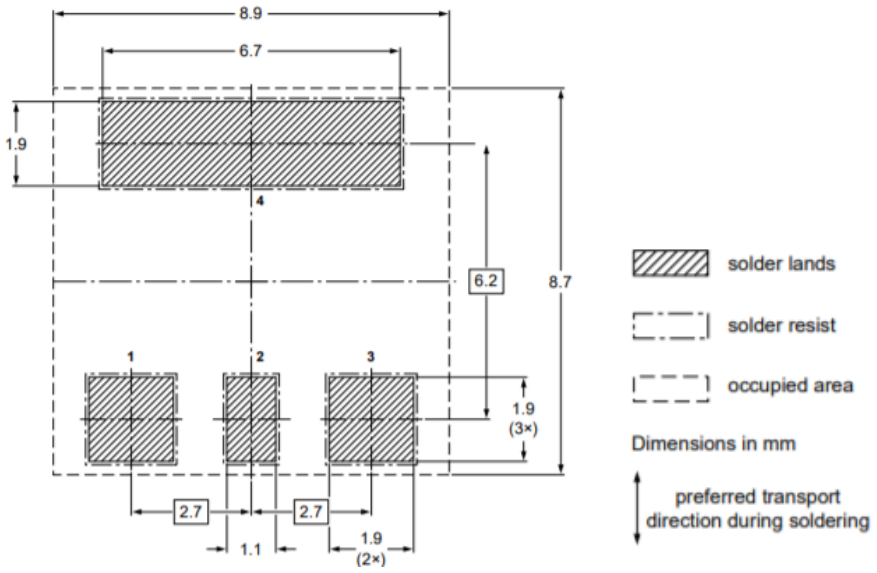


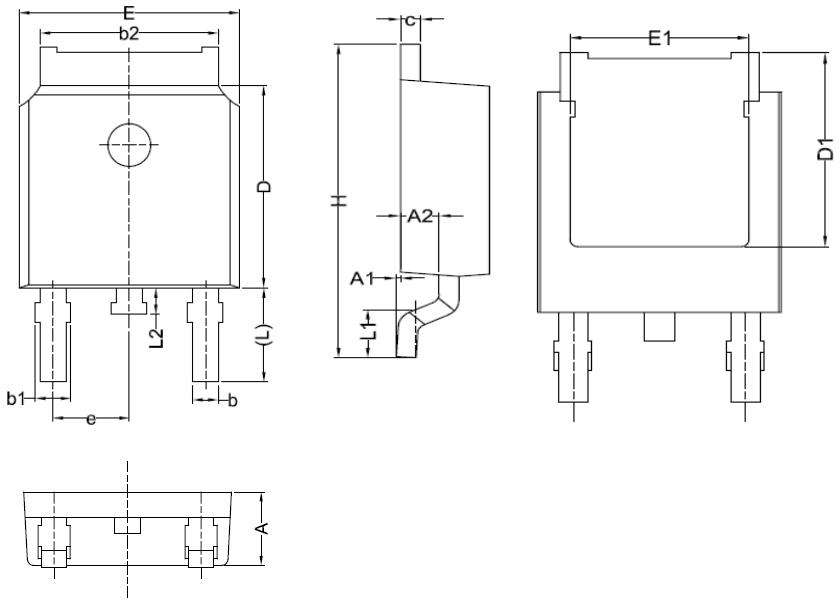
Fig.3 SOT223 solder lands layout for wave soldering

4. TO252

TO252 (Fig. 4), also known as SOT428 and DPAK, is a plastic SMT package which occupies an area on the PCB that is not much larger than the area required for the SOT223 package. It can be soldered to a universal SOT223 and TO252 pad layout. Fig. 5 and Fig. 7 show the pad and relative component sizes. The main pad area of 20 mm^2 is the minimum practical pad size for TO252. TO252 has three legs, which emerge from one edge of the plastic body. The centre leg is cropped off close to the plastic and is not used for electrical connection. The "centre leg connection" is made from the device's metal mounting base to the main PCB pad. The two outer legs are formed to bring them into contact with the PCB pads for soldering.

4.1 TO252 soldering

This surface-mount package features a relatively large solder area (compared to SOT223), which is hidden after assembly. In this case, wave soldering cannot be relied upon to wet the joint sufficiently because the meeting surfaces between the main PCB pad and the device are hidden. It is therefore necessary to use a reflow soldering method for packages of this design. Fig. 6 shows typical TO252 solder pad dimensions.



Unit	A	A1	A2	b	b1	b2	C	D	D1	e	E	E1	H	L	L1	L2
Min (mm)	2.20	0.00	0.90	0.71	0.72	5.23	0.47	5.98	5.25	2.285 typ	6.47	4.7	9.6	2.9 (ref)	1.40	0.5
Max (mm)	2.38	0.10	1.10	0.89	1.10	5.43	0.60	6.22	-		6.73	-	10.4		1.70	1.0

Fig. 4 Package outline for TO252

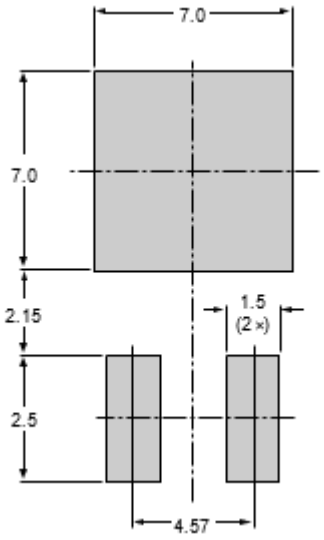


Fig. 5 TO252 pad layout for reflow soldering

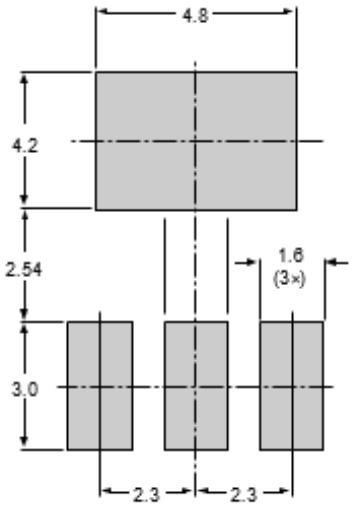


Fig. 6 SOT223 and TO252 universal pad layout

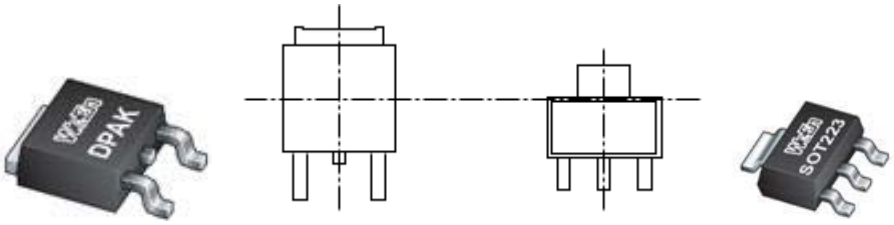


Fig. 7 TO252 and SOT223 relative package sizes

4.2 TO252 design features and surface mounting

It is well known among power semiconductor manufacturers that the larger a surface mounted power semiconductor is, the more vulnerable it is to die stresses during manufacture and during the surface mounting process. This can result in a significant percentage of rejects due to die cracking.

Experience has shown that it is not possible to use the same manufacturing techniques for surface-mount devices as are used for through-hole devices. Unacceptable failure rates will certainly be the result, either during manufacture, during surface mounting or during prolonged thermal cycling in the application.

WeEn Semiconductors has spent a long time perfecting its TO252 package before releasing it onto the market so that these pitfalls can be avoided. Described below are some of the special design features that ensure successful manufacture and long-term reliable operation in the customer's application.

- The package is moulded using a low stress epoxy plastic to minimize the bending force on the mounting base as curing takes place. Less bending of the mounting base means less die stress.
- A thick copper mounting base of 0.93 mm maximum thickness is used to further inhibit any tendency for bending of the mounting base.
- A low stress soft solder is used for die bonding. The amount of "give" in the solder accommodates differential expansions and minimizes die stress
- A new technique has been developed to accurately control the thickness and positioning of the die-attach solder on the die pad. This guarantees optimum die bonding over the complete die area every time without unsoldered areas or excess solder. The benefit of this is to offer the best long-term reliability under thermal stress and the minimum junction-to-mounting base thermal resistance
- Special locking features are used to lock the epoxy to the metal to improve hermeticity. These features have been carefully optimized to provide good hermeticity while avoiding excessive die stress during differential expansion.
- A bare copper die pad is used for best adhesion of the epoxy to the metal. This promotes good hermeticity.

- The footprint is compatible with JEDEC industry standard layouts.
- The co-planarity of leads to seating plane and leads to leads meets stringent industry standards.
- A fully automatic high-volume production line is used which takes in the raw components at its input and delivers assembled, 100 % tested, packaged devices at its output.
- All assembled devices are subjected to an in-line surface-mount temperature profile pass to eliminate any remaining possibility, however small, of zero-hour defects at the customer.
- Devices are packaged in industry standard blister pack reels for loading onto automatic pick-and-place machines.

5. TO263

TO263, as shown in Fig.9, (also known as SOT404 and D^2PAK) possesses the same size of plastic body as TO220 (SOT78). The similarity ends there. TO263 is manufactured without a tab since no mounting hole is required. (It is not merely a cropped TO220!) The centre lead is cropped close to the plastic, so the "centre leg connection" is made via the metal mounting base. The two outer leads are formed downwards to bring them into contact with the PCB.

5.1 TO263 soldering

As for TO252 (SOT428), it is also not possible to solder TO263 using a wave soldering technique. The even larger body and larger hidden solder area would put this method out of the question. Reflow soldering is essential. Fig. 8 shows typical TO263 solder pad dimensions.

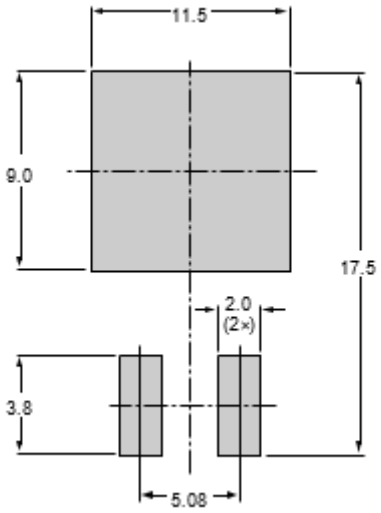
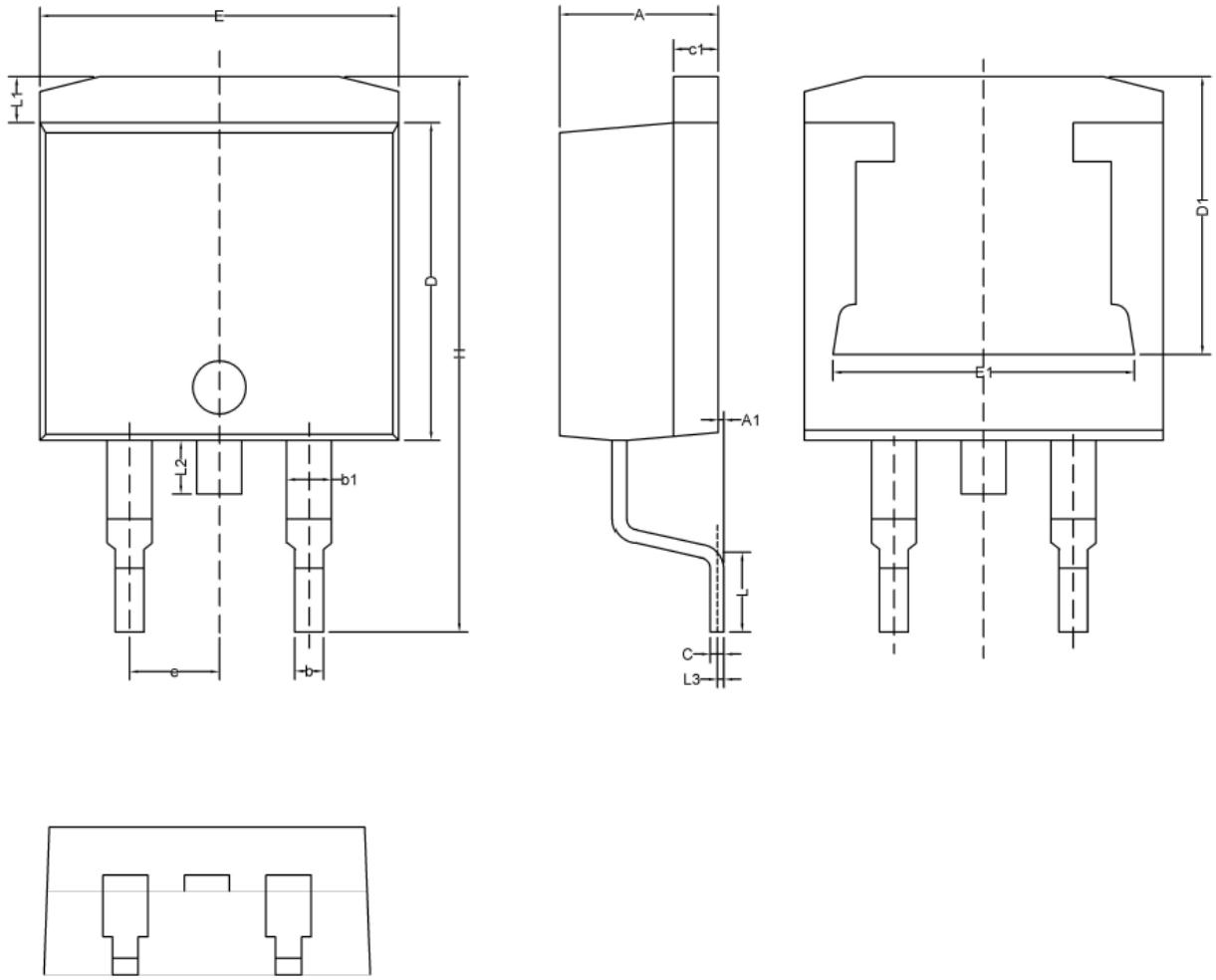


Fig. 8 TO263 pad layout for reflow soldering

In designing and manufacturing the TO263 package, similar measures must be taken as for TO252 to ensure a reliable manufactured product. These include:

- A low stress epoxy to minimize bending forces on the mounting base after curing (minimizes die stress).
- A thick copper mounting base of 1.4 mm (0.055 inch) max thickness to further minimize any tendency to bend.
- A low stress soft die bond solder (minimizes die stress).
- Accurate dosing and spreading of the die-attach solder prior to die bonding to ensure optimum die bonding over the complete die area every time without unsoldered areas or excess solder. This offers best long-term reliability under thermal cycling and optimum junction-to-mounting base thermal resistance.
- Optimized locking features to balance the conflicting requirements of good hermeticity with enough differential movement to avoid die stress fracture.
- A bare copper die pad to ensure good epoxy-to-metal adhesion for best hermeticity.
- Compatibility with the industry standard footprint layout for TO263 (D^2PAK).
- Co-planarity check on leads to seating plane and leads to leads.
- A specially designed leadframe to reduce cropping forces as each device is separated from the comb. This avoids die cracking due to shock loading.
- A surface-mount temperature profile pass to eliminate zero-hour defects at the customer.

- Devices are packaged in industry standard blister pack reels for loading onto automatic pick-and-place machines.

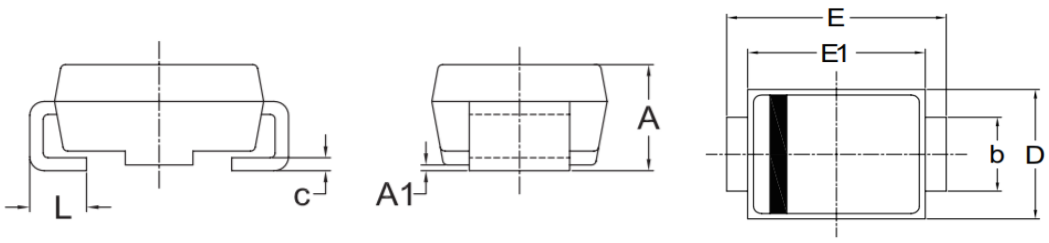


Unit	A	A1	b	b1	c	C1	D	D1	E	E1	e	H	L	L1	L2	L3
Min (mm)	4.35	0	0.69	1.14	0.38	1.14	8.5	7.5	10.0	8.25	2.54 (BSC)	14.6	2.5	1.0	1.27	0.25 (BSC)
Max (mm)	4.75	0.15	0.99	1.73	0.61	1.40	9.02	8.0	10.4	8.80		15.6	2.79	1.65	1.78	

Fig. 9 Package outline for TO263

6. SMA (DO-214AC)

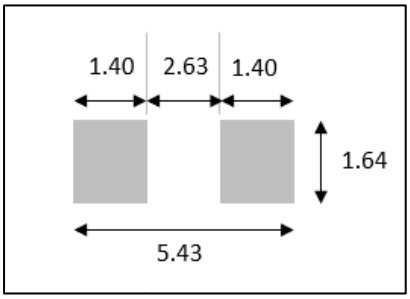
SMA is the smallest surface mount package in the SMx family used to package diodes.



UNIT (mm)	A	A1	b	c	D	E	E1	L
max	2.35	0.20	1.50	0.31	2.80	5.20	4.45	1.50
min	1.95	0.05	1.30	0.15	2.50	4.80	4.15	0.90

Remark: Dimensions D and E1 do not include mold flash

Fig. 10 Package outline for SMA

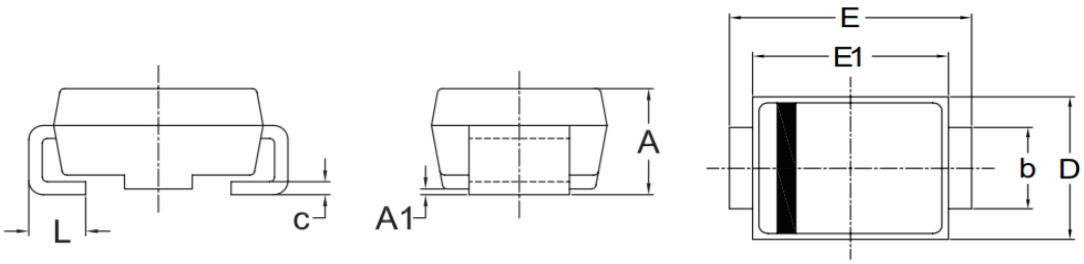


Dimensions in mm

Fig. 11 SMA pad layout

7. SMB (DO-214AA)

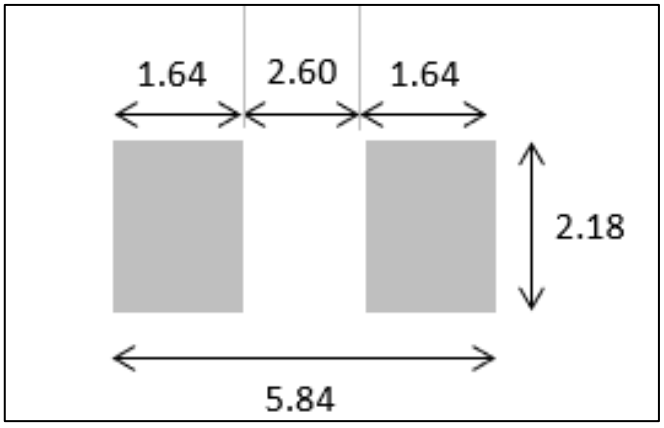
SMB is the middle-sized surface mount package in the SMx family used to package diodes.



UNIT (mm)	A	A1	b	c	D	E	E1	L
max	2.50	0.20	2.21	0.31	3.95	5.6	4.60	1.60
min	2.00	0.05	1.96	0.15	3.30	5.2	4.05	0.75

Remark: Dimensions D and E1 do not include mold flash

Fig. 12 Package outline for SMB

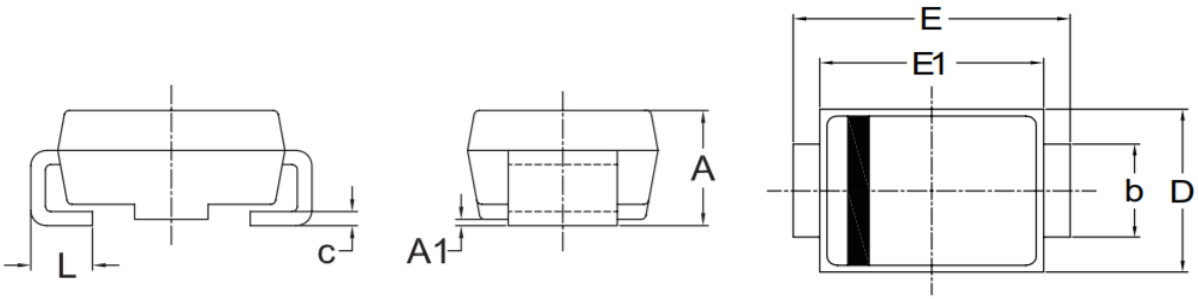


Dimensions in mm

Fig. 13 SMB pad layout for reflow soldering

8. SMC (DO-214AB)

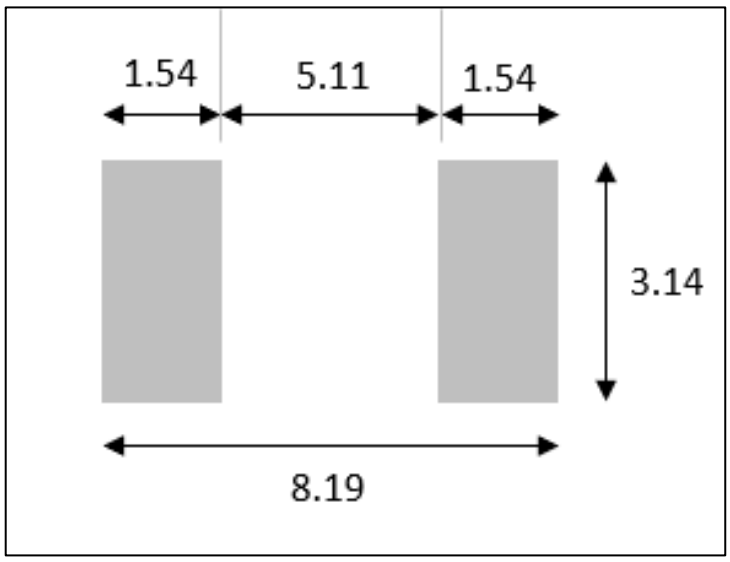
SMC is the largest surface mount package in the SMx family used to package diodes.



UNIT (mm)	A	A1	b	c	D	E	E1	L
max	2.40	0.22	3.18	0.31	6.22	8.13	7.11	1.52
min	2.01	0.05	2.92	0.15	5.59	7.70	6.60	0.76

Remark: Dimensions D and E1 do not include mold flash

Fig. 14 Package outline for SMC

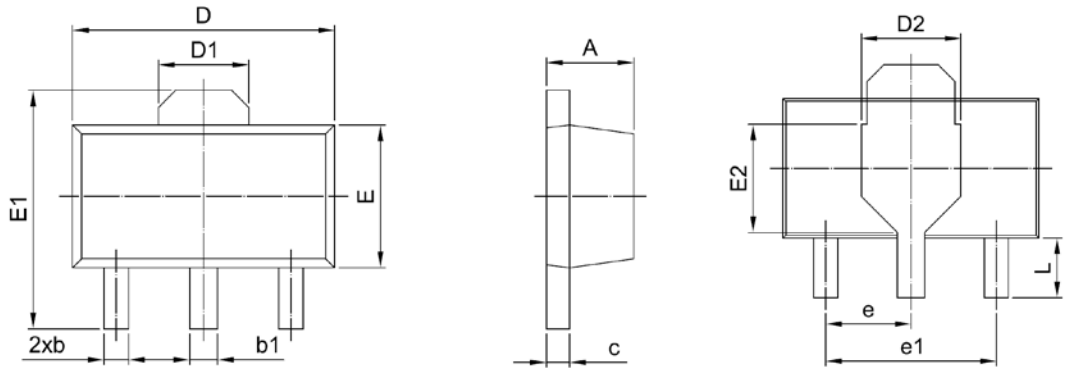


Dimensions in mm

Fig. 15 SMC pad layout for reflow soldering

9. SOT89

SOT89 is a small surface mount package of 3 leads with a tab heatsink attached to the centre lead.



UNIT (mm)	A	b	B1	c	D	D1	D2	E	E1	E2	e	e1	L
min	1.35	0.32	0.40	0.30	4.35	(1.55)	(1.75)	2.30	3.85	(1.90)	1.50 (typ)	3.00 (typ)	0.85
max	1.65	0.52	0.60	0.50	4.65			2.60	4.35				1.25

Fig. 16 Package outline for SOT89

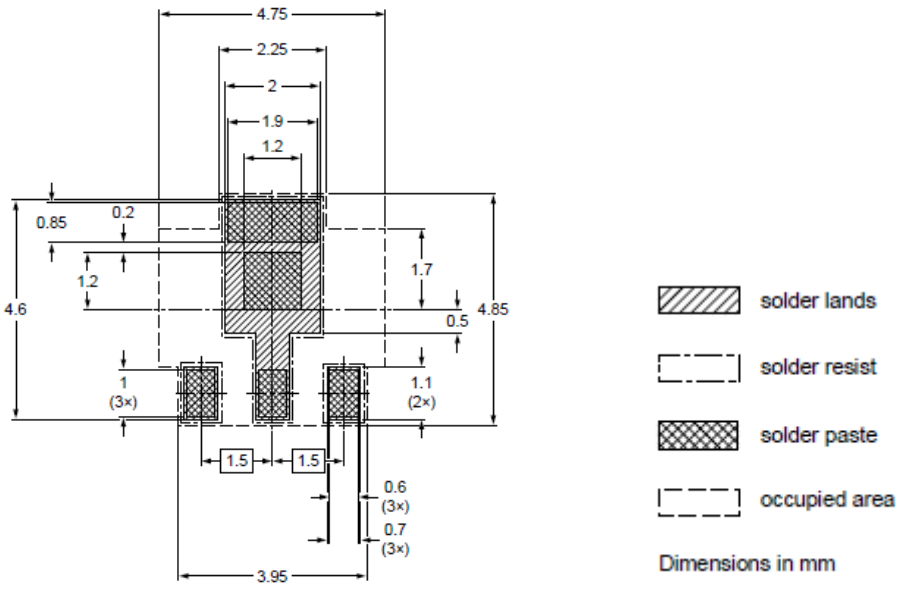


Fig. 17 SOT89 pad layout for reflow soldering

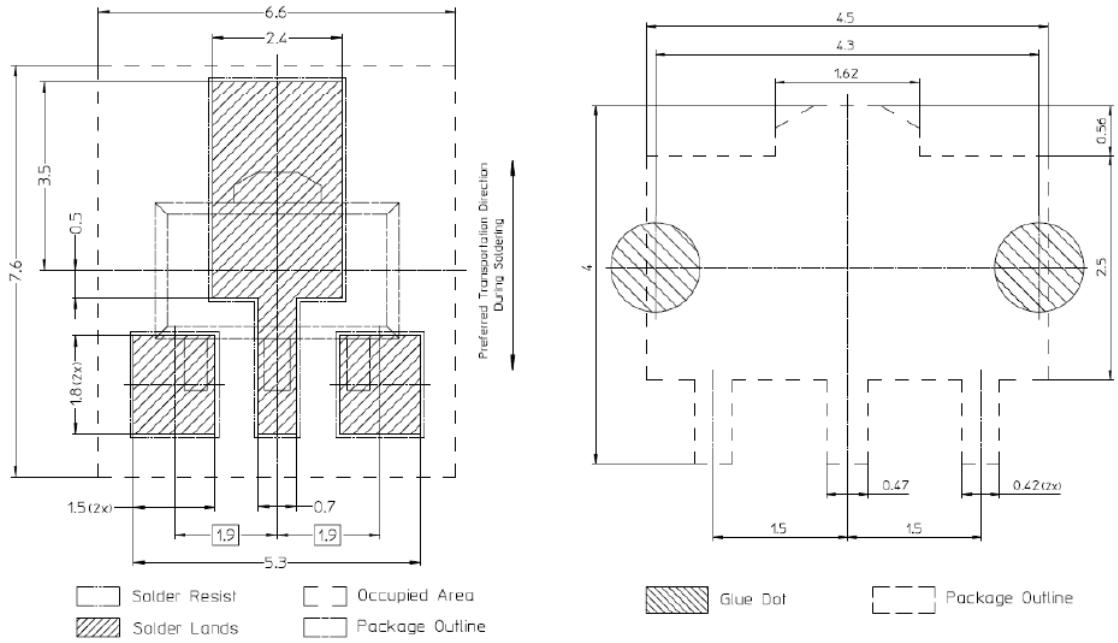
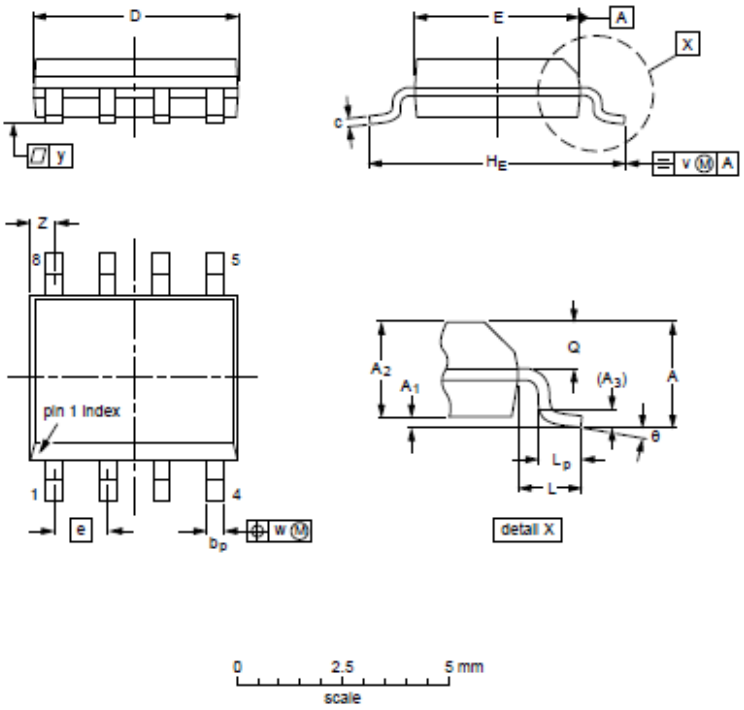


Fig. 18 SOT89 solder land layout and glue dot layout for wave soldering

10. SO8 (MS-012)

The SO8 package is a plastic, small outline package with 8 leads of 1.27 mm pitch.



Unit (mm)	A max	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
max	1.75	0.25	1.45	0.25	0.49	0.25	5.00	4.00	1.27	6.20	1.05	1.00	0.70	0.25	0.25	0.10	0.70	8°
min		0.10	1.25		0.36	0.19	4.80	3.80		5.80		0.40	0.60	0.01	0.10		0.30	0°

Notes:
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

Fig. 19 Package outline for SO8

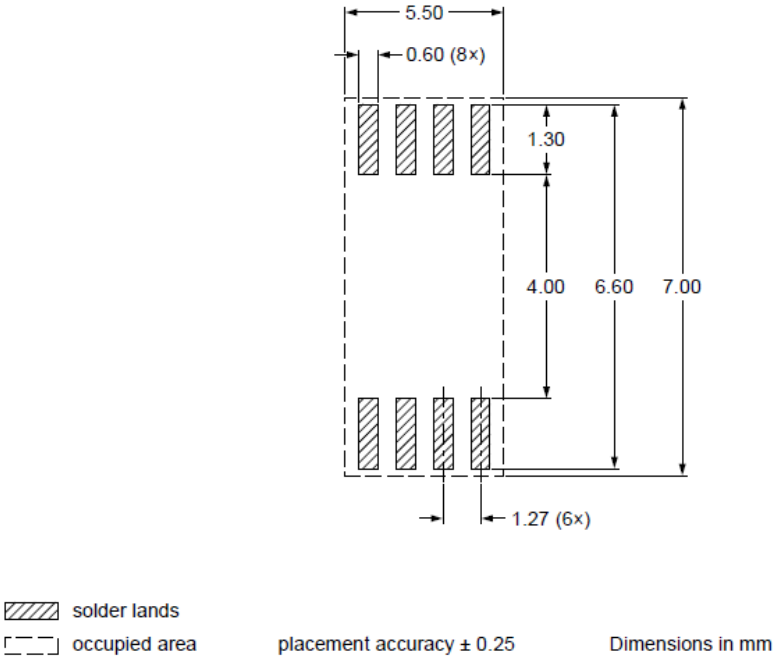


Fig. 20 SO8 pad layout for reflow soldering

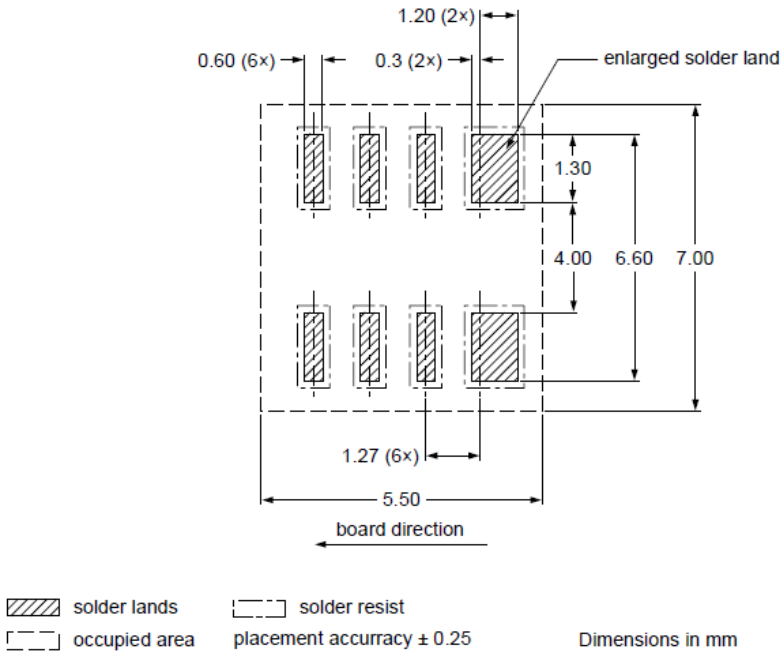


Fig. 21 SO8 solder lands layout for wave soldering

11. Mounting and soldering

The SM footprint drawings define the solder land (pad) areas, the solder resist areas and the area occupied by the package. Since the solder lands must be completely free of solder resist, the areas without the solder resist are always slightly greater than the solder land areas. The solder resist must cover all areas of the PCB that are not soldered to. This includes extended areas of copper used for heatsinking.

The footprints for reflow soldering define the solder paste areas in addition to the areas listed above. Solder paste is applied using a metal stencil which must be accurately aligned to within 0.1 mm over the pads. A metal "squeegee" is drawn across the stencil to deposit the paste through the apertures, which must be the same size as the solder paste areas defined on the footprint drawings. With reference to Fig. 2 and Fig. 3, the optimum pad areas are different for wave soldering and for reflow soldering.

When wave soldering, surface-mount devices must be held in position by a small measured dose of glue. A double wave process is used to ensure better wetting of all joints without solder shadows. Wave soldering **must** be used if there are any through-hole components on the PCB.

During reflow soldering, surface-mount devices are held in position by the viscosity of the solder paste. When the solder is melted in the reflow oven, the surface tension of the molten solder causes them to self-centre on their pads. The pad sizes and configuration are critical if self-centring is to operate reliably.

Both soldering methods are sometimes employed on PCBs containing a mixture of surface-mount and through-hole components, to ensure optimum soldering of both technologies.

A more detailed description of the wave and reflow soldering processes is beyond the scope of this application note.

Flatpack packages are not usually recommended for wave soldering because they do not have a standoff height like gullwing packages (see Fig. 22).

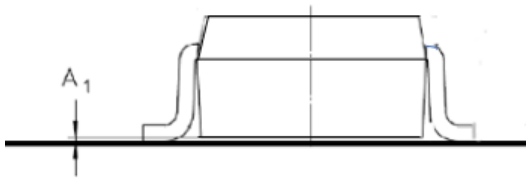


Fig. 22 Gullwing package with stand-off height from PCB of approx. 50µm

For wave soldering the plastic body of the packages needs to be fixed with glue prior to the wave solder process. Unlike gullwing packages, the plastic body of flatpacks is directly touching the PCB surface. Consequently, there is no space for the volume of glue under the plastic body. This brings a risk that the glue will be squeezed out to contaminate the solder pads so that the wetting of the liquid solder is frustrated. This may lead to inadequate solder quality. The risk increases the smaller the flatpack package. This is the background as to why WeEn does not recommend the wave soldering process for flatpacks.

However, if a customer wishes to apply wave soldering for flatpacks- even although it is not optimal- it is at their own risk. Due to the variety of PCB designs, surface finishes and glues that can be used, WeEn Semiconductors cannot guarantee wave soldering quality for all these differing circumstances.

The SOT89 package is suitable for reflow soldering and can be utilized for wave soldering but the solder pads must be larger. This is because for wave soldering the pads must act as solder catchers. The wetting with solder needs to start from the solder pads and the component leads are then wetted from these pads.

It is important that the glue volume should be reduced to a minimum. Two small glue dots should be applied, instead of a large one in the centre of the device, to avoid excessive glue squeezing on the solder pads. This glue technique is also recommended for gullwing SMD packages (see Fig. 18).

To give the glue some room under the plastic body of a flatpack, dummy tracks of the PCB can be designed under the plastic body of the component. The copper track can then be etched away and provided there is an opening in solder resist, a trench underneath the plastic body can be generated. A similar “trench effect” can be achieved with non-solder mask defined (NSMD) tracks. This method of designing either normal or dummy tracks underneath a component is a well-known method to balance surface topography differences of a PCB.

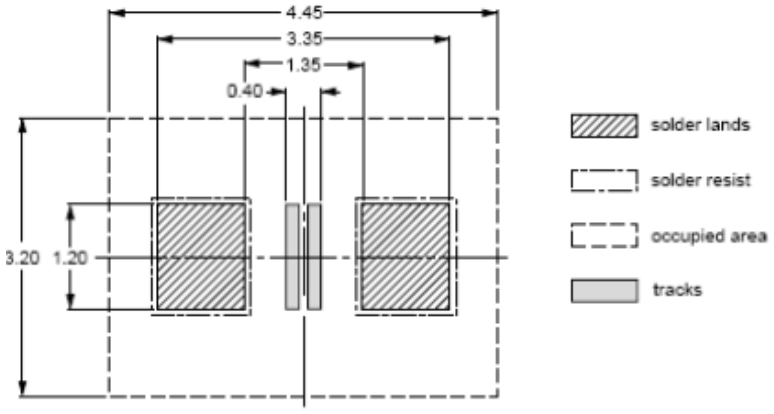


Fig. 23 Example of dummy copper tracks under plastic body of component

12. Thermal resistance

Detailed tests have been conducted on the junction-to-ambient thermal resistance $R_{th(j-a)}$ of the SOT223, TO252 and TO263 surface mount packages when mounted to different pad sizes on standard FR4 PCB. The repeatability of the test results gives a high level of confidence in their validity.

12.1 Theory

It is possible to measure the temperature of a power semiconductor junction by measuring one of its temperature-dependent characteristics. With a MOSFET for example, it might be the forward voltage of the anti-parallel diode and for a thyristor it would be the on-state voltage (V_T). To heat up the device under test, a heating current is passed through it. When measuring its temperature-dependent characteristic, a much lower calibration current is passed for a very short measurement period.

SCRs were used for this investigation because of the relative ease of measurement.
(SCRs only must be measured in one direction, whereas triacs have to be measured in forward and reverse directions and the results combined.)

The size of the die within any given package will not affect the final $R_{th(j-a)}$ result appreciably because any differences in the junction-to-case thermal resistance $R_{th(j-c)}$ will be insignificant compared to the case-to-ambient thermal resistance $R_{th(c-a)}$. Therefore, it is not critical which device is used when measuring package R_{th} in free air or when surface mounted to conventional PCBs with relatively high thermal resistances to ambient.

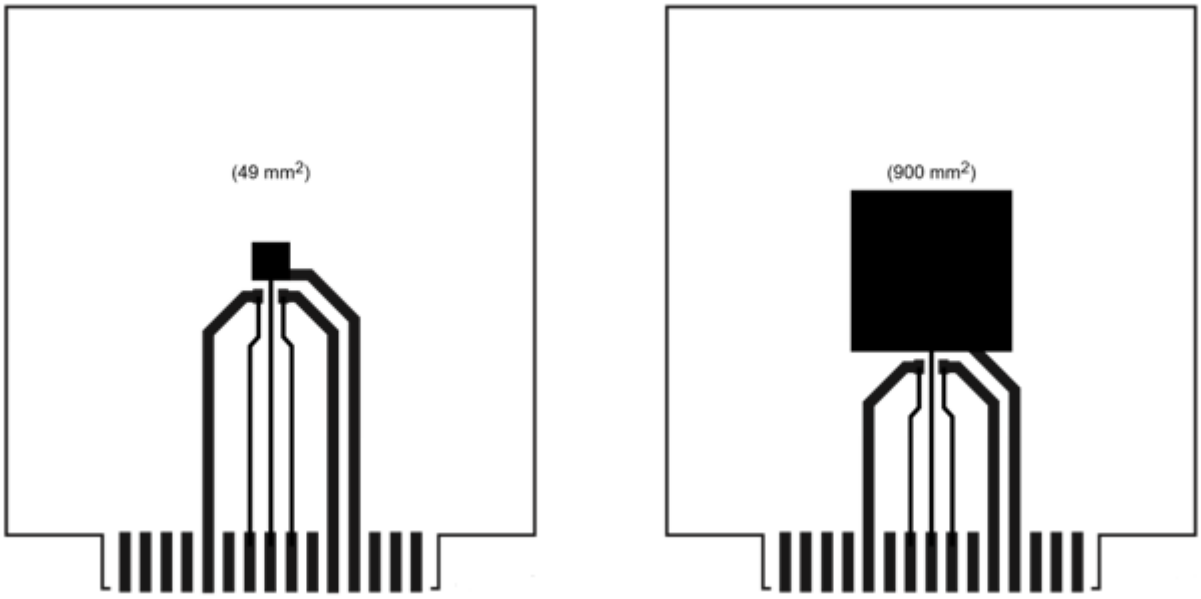
FR4 fiberglass PCB with 35 µm copper (1 oz/square foot) was used because it is an industry standard to which everyone can relate. It is the PCB type that is always quoted in power semiconductor manufacturers' data sheets. It has become a "reference standard" by default. Despite this "standard" status, many industries cannot justify its use because of its cost. The home appliance industry prefers to use a lower cost alternative, one example of which is CEM3. This is a resin and paper-based material with fibre on both sides. Fortunately, the thermal performance of the cheaper alternatives is sufficiently close to that of FR4 in many cases to make the results of this investigation valid for those also.

12.2 Equipment

The test PCBs had pad sizes that varied upwards from the minimum recommended for the package. Consistent pad width: height ratios were maintained. The pad was always positioned centrally on the test board to assure consistent heatsinking to the bulk of the PCB. SOT223 and TO252 used the same pad layouts, while TO263 had its own PCBs.

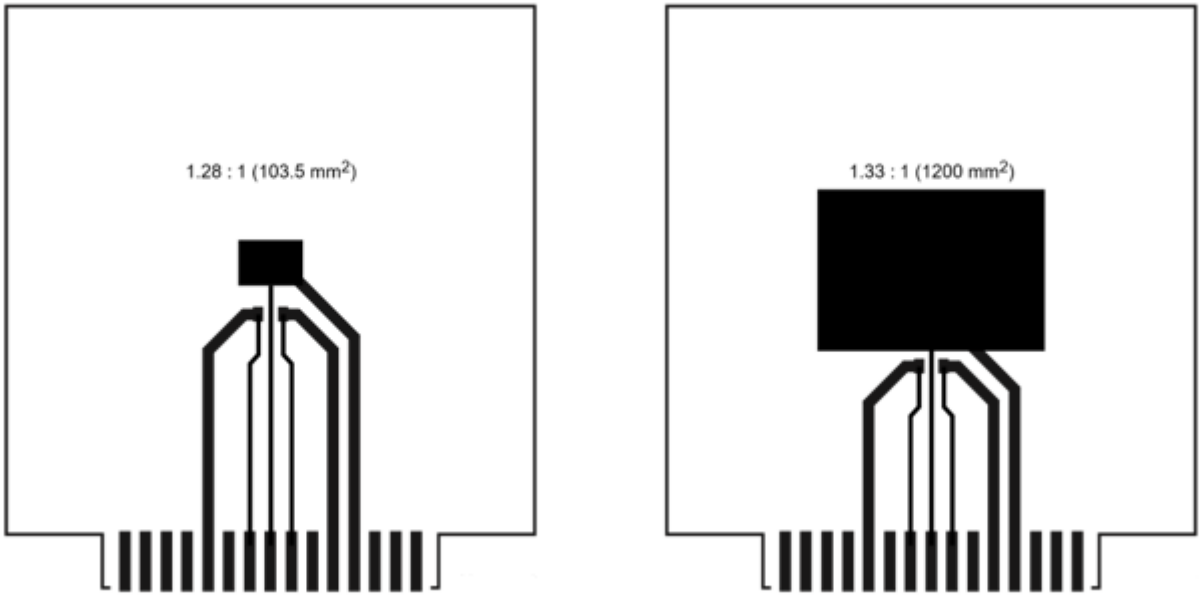
Fig. 24 shows the second smallest and largest pad size test boards for SOT223 and TO252, and Fig. 25 shows the smallest and largest pad size test boards for TO263.

Remark: The following test boards are not shown at 1:1 scale.



(i) Small pad area (ii) Large pad area

Fig.24 SOT223 and TO252 test PCB layout



(i) Small pad area (ii) Large pad area

Fig.25 TO263 test PCB layout

Separate power and measurement connections were taken via an edge connector to the device. The PCBs were standard fiberglass FR4 with 35 µm copper, which had been very lightly "tinned" by electrochemical deposition. (Thermal resistance will not be reduced by a thick layer of roller tinning.) The PCBs were made relatively large at 100 mm × 100 mm to ensure that R_{th} is controlled by pad area and not by PCB area.

SCRs were tested using a custom-built thermal resistance test gear. (SCRs were tested in preference to triacs because they only require one measurement for each power setting, whereas triacs need measuring in both directions with the average power being calculated from the results.)

The most important fact to remember when conducting the tests was that they take a lot of time. It was essential to ensure that thermal equilibrium and stability had been reached before readings were taken at elevated device temperature. Rushing the tests would give incorrect results and improbable graphs.

12.3 Results

The resolution and accuracy of the final $R_{th(j-a)}$ results were maximized by generating high values of ΔT_j, hence large measured voltage variations (ΔV). The results tables show $R_{th(j-a)}$ (K/W) versus power dissipation and pad area. The power levels highlighted with table notes indicate a suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB. (In the case of the SOT223 package, the smallest pad area used was 20 mm^2. This area is fully occupied by the TO252 package. The minimum for SOT223 is 5.7 mm^2. Therefore the 1 W power dissipation achieved in these experiments will be higher than that achievable with a 5.7 mm^2 pad. 0.5 W is likely to be the practical maximum power dissipation for SOT223 on a 5.7 mm^2 pad.)

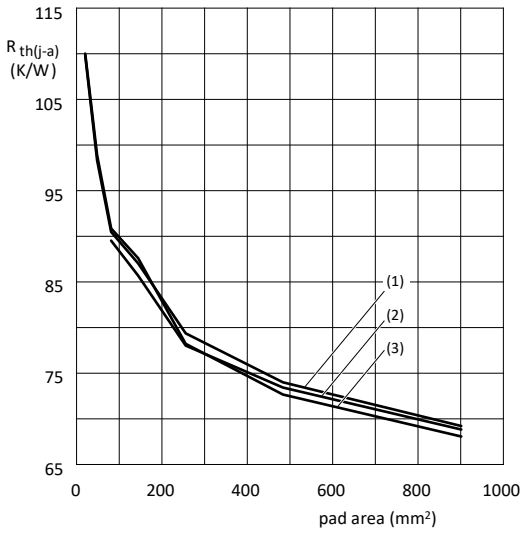
The results graphs show $R_{th(j-a)}$ versus pad area and ΔT_j versus pad area. With any given package, higher power dissipation leads to higher ΔT_j, which in turn leads to lower $R_{th(j-a)}$. This is because a larger temperature difference results in more efficient radiation to ambient.

Table 1. SOT223 thermal characteristics

SOT223 $R_{th(j-a)}$ vs pad area and power dissipation.

Area (mm^2)	0.5W	1.0W [1]	1.5W
20	110	110	-
49	99	98	-
81	91	90	90
144	88	87	86
256	78	79	78
484	73	74	73
900	68	69	69

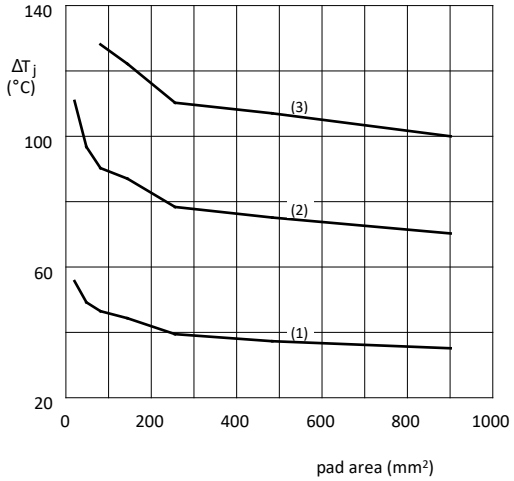
[1] The suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 0.5W
(2) 1.0W
(3) 1.5W

Fig.26 SOT223 $R_{th(j-a)}$ vs PCB pad area



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 0.5W
(2) 1.0W
(3) 1.5W

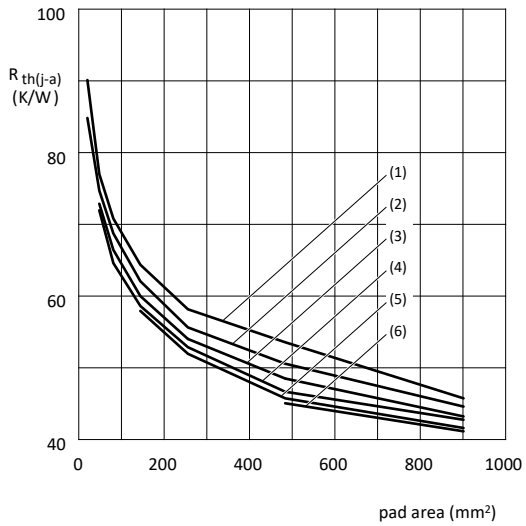
Fig.27 SOT223 junction temperature rise vs PCB pad area

Table 2. TO252 thermal characteristics

TO252 $R_{th(j-a)}$ vs pad area and power dissipation

Area (mm^2)	0.5W	1.0W [1]	1.5W [1]	2.0W	2.5W	3.0W
20	90	85	-	-	-	-
49	77	75	73	72	-	-
81	71	69	66	65	-	-
144	64	62	60	59	58	-
256	58	56	54	53	52	-
484	54	50	48	47	46	45
900	46	45	43	43	42	41

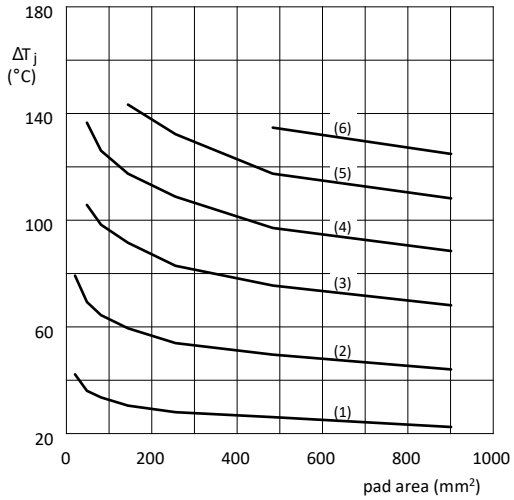
[1] The suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 0.5W
(2) 1.0W
(3) 1.5W
(4) 2.0W
(5) 2.5W
(6) 3.0W

Fig.28 TO252 $R_{th(j-a)}$ vs PCB pad area



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 0.5W
(2) 1.0W
(3) 1.5W
(4) 2.0W
(5) 2.5W
(6) 3.0W

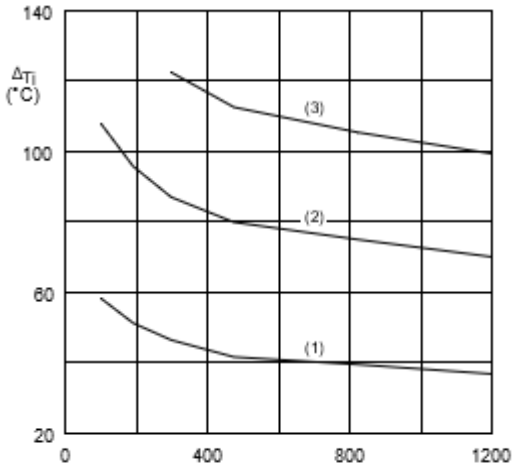
Fig.29 TO252 junction temperature rise vs PCB pad area

Table 3. TO263 thermal characteristics

TO263 $R_{th(j-a)}$ vs pad area and power dissipation

Area (mm^2)	1.0W [1]	2.0W [1]	3.0W [1]
103.5	60	55	-
192	52	47	-
300	47	43	41
475	41	39	37
825	39	36	34
1200	36	34	32

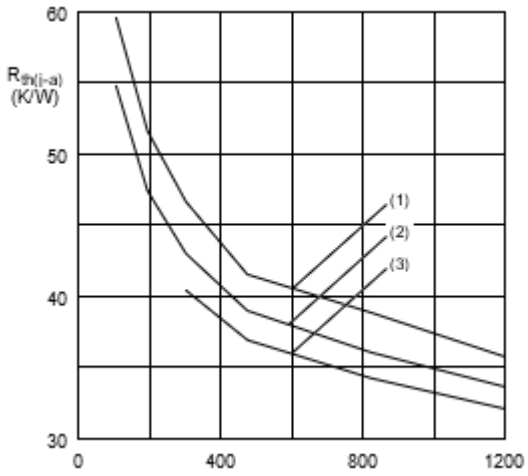
[1] The suggested power dissipation limit for the package when soldered to the minimum pad area on FR4 PCB



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 1.0W
(2) 2.0W
(3) 3.0W

Fig.30 TO263 $R_{th(j-a)}$ vs PCB pad area



100 × 100 mm FR4 PCB positioned vertically in still air.

(1) 1.0W
(2) 2.0W
(3) 3.0W

Fig.31 TO263 junction temperature rise vs PCB pad area

13. Conclusion

The maximum practical power dissipations are summarized below for stagnant ambient conditions at 25 °C. These are for standard FR4 PCB or similar without special heatsinking provisions. The 35 µm copper had been lightly tinned by electrochemical deposition.

Table 4. Overview of package characteristics

Package	P_{max} (W)	Pad area (mm^2)	ΔT_j (°C)	$R_{th(j-a)}$ (K/W)	
				Experimental	**Specified in data**
SOT223	1.0	20	97	99	**156** (5.7mm^2 pad)
		650	74	72	**70** (648mm^2 pad)
TO252	1.0 < 1.5	20	106	73	**75**
TO263	2.0	104	108	55	**55**

SOT223 and TO252 can be soldered to common pad layouts. 20mm^2 was the absolute minimum pad area for soldering TO252. The reasonable power dissipation for TO252 on 20mm^2 fell somewhere between 1.0W and 1.5W.

The minimum pad quoted in data for SOT223 is 5.7mm^2. 0.5W is the more realistic maximum power dissipation for SOT223 on its minimum pad.

Revision history

Rev	Date	Description
v.1	20090722	New format update

Contact information

For more information and sales office addresses please visit: http://www.ween-semi.com

Legal information

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. WeEn Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, WeEn Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. WeEn Semiconductors takes no responsibility for the content in this document if provided by an information source outside of WeEn Semiconductors.

In no event shall WeEn Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, WeEn Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of WeEn Semiconductors.

Right to make changes —WeEn Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — WeEn Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an WeEn Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. WeEn Semiconductors and its suppliers accept no liability for inclusion and/or use of WeEn Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. WeEn Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using WeEn Semiconductors products, and WeEn Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the WeEn Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third-party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

WeEn Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third-party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using WeEn Semiconductors products to avoid a default of the applications and the products or of the application or use by customer's third-party customer(s). WeEn does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. WeEn Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall WeEn Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of WeEn Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

For more information, please visit: http://www.ween-semi.com

Date of release: 22 July 2019 Document identifier: WAN007