1 Introduction

Silicon carbide (SiC) MOSFETs have made significant progress in the power semiconductor, making them received more and more attention. Compared with traditional silicon-based devices, SiC MOSFETs have smaller on-resistance and fast switching speed, especially the conduction loss and switching loss are significantly reduced compared with silicon IGBTs. The use of SiC MOSFET devices brings hope for further improvement of actual system efficiency and further reduction of system volume. However, SiC MOSFETs also bring a lot of challenges in applications, such as Miller effect, short circuit, electromagnetic interference and so on.

Therefore, as an important part of controlling the switching power device on and off, the gate driver selection and design is also a key point in system applications. A suitable gate driver selection and design can not only play the advantages of SiC MOSFETs, but also solve the challenges bring by SiC MOSFETs.

This Application Note provides SiC MOSFETs features, describes tis benefits and explain how to choose the suitable gate driver for SiC MOSFETs.

1.1 Definitions/Abbreviations

SiC	Silicon Carbide
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
Si	Silicon
EAS	Avalanche Energy for Single pulse
Vpos	Positive Voltage
Vneg	Negative Voltage
OCP	Over Current Protection

2 SiC MOSFET Features

Outstanding features of WeEn's SiC MOSFET can be found as below:

- Lower conduction losses: G2 Ron.sp can achieve 3.1 mΩ*cm^2 and G3 Ron.SP can achieve 2.2 mΩ*cm^2 which is very competitive. The detail can see in Fig. 1.

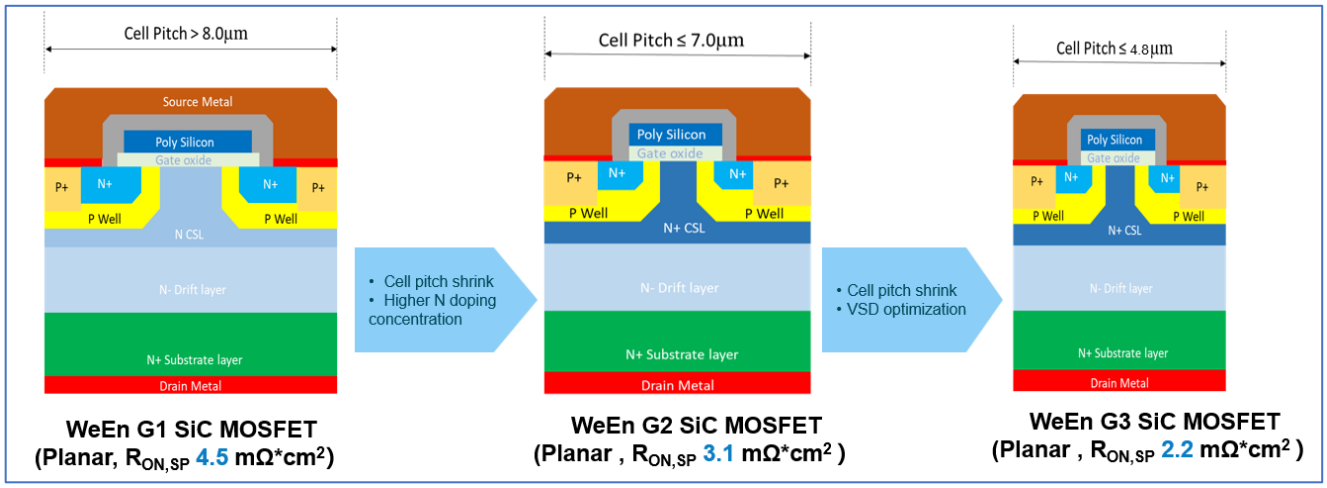


Fig. 1. The chip technology generation roadmap

- Higher usability: Optimized gate oxide to ensures the device operates normally under 15V or 18V gate driving voltage which makes it easier to be adopted in more traditional designs.
- Higher gate robustness: The permission range of voltage between gate and source is from -12V to 24V for industrial products and from -10V to 22V for automotive products. Which also tested in reliability test to ensure gate robustness.
- Excellent thermal performance: Using Ag sintering technology can reduce the thermal resistance; The excellent on resistance temperature stability makes Lower Rdson increase at high temperatures than competitor. The detail can see in Fig. 2.

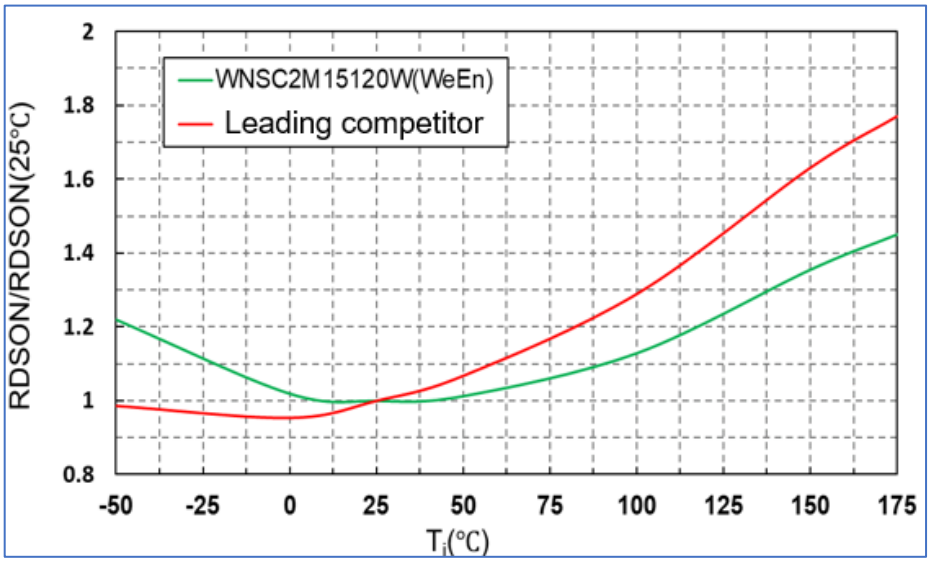


Fig. 2. Drain source on state thermal performance

2.1 V_{DS} & $V_{GS,max}$

V_{DS} and $V_{GS,max}$ are important parameters to evaluate the performance of SiC MOSFET. And they are also as boundary conditions in driver circuit design, the detail can see chapter 3.3. The data V_{DS} and $V_{GS,max}$ are usually given in the datasheet. Fig 3 shows related parameters, using WeEn SiC MOSFET as example.

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		1200	V
$V_{GS,max}$	gate-source voltage			-12 to 24	V
$V_{GS,op}$	gate-source voltage			-4 to 18	V

Fig. 3. Example of related characteristics.

V_{DS} is the maximum allowable instantaneous off-state voltage (including transients) that the circuit can apply between the drain and source of the SiC MOSFET when the gate is shorted to the emitter between 25°C and 175°C. If V_{DS} is exceeded there may be damage caused to the SiC MOSFET depending on the circuit conditions.

Usually, the V_{DS} value has a positive correlation with the temperature, so the lower the temperature the lower the V_{DS} value. The SiC MOSFET will not be immediately damaged if the drain-source voltage rises above limitation, it will only be damaged if the avalanche breakdown energy EAS exceeds the allowable value specified in data.

$V_{GS,max}$ shows the permissible range of voltage between gate and source that can be applied without degradation or permanent damage to the device.

$V_{GS,op}$ shows the range for normal operation of the device. It is useful for defining the gate driver supply voltage design. This is an optimization recommendation based on comprehensive consideration of performance and reliability in system application. The detail can see chapter 3.2.

For WeEn's SiC MOSFET, it is also supported -5V~0V of negative gate voltage and +15V~+18V of positive gate voltage in system application. Due to the widely $V_{GS,max}$ allowed.

2.2 $V_{GS\,(th)}$ & R_G

The gate-source threshold voltage, $V_{GS\,(th)}$ is specified for a leakage current that was chosen because of its relationship to the drain current density and the active area of the device.

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	I_D = 10 mA; V_{DS} = 10 V; T_j = 25 °C		1.9	2.6	3.5	V
		I_D = 10 mA; V_{DS} = 10 V; T_j = 175 °C		-	1.9	-	V
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		-	1	-	Ω

Fig.4. Example of related characteristics.

$V_{GS\,(th)}$ reduces with increasing temperature. The minimum value of $V_{GS\,(th)}$ at high temperature is an important parameter in system design for the following reason:

When the MOSFET's VDS rises rapidly, a displacement current will be generated to charge the Miller capacitance C_{GD}. Consequently, a voltage spike will appear on the gate when the current passes through R_G (R_G= R_{G_EXT} + R_{G_IN}). If the voltage spike is higher than $V_{GS\,(th)}$, the MOSFET will be turned on mistakenly, causing

a serious short circuit problem. So, a safe margin is necessary to prevent mistaken turn-on caused by the Miller effect, as shown in chapter 3.4.

Gate resistance R_G is the inherent resistance on the element's gate wiring. In general, for the same structure of SiC MOSFET, the smaller the die size, the higher the internal gate resistance. When driving the gate of a MOSFET, the external gate resistance (R_{G_EXT}) and the internal gate resistance (R_{G_IN}) are connected in series between the gate driver and the gate oxide film. Therefore, the smaller the "sum" of R_{G_EXT} and R_{G_IN}, the faster the switching speed and the smaller the switching loss.

For WeEn's SiC MOSFET, the design of R_{G_IN} is small. As a result, R_{G_EXT} has a larger tuning range. This allows the device to flexibly respond the gate surge suppression and switching speed improvement.

2.3 Capacitance Characteristics

The Capacitance characteristics are important to consider in gate drive design and the switching behaviour of the SiC MOSFET. Fig 5 showing the relationship of the measured typical capacitance values for C_{iss}, C_{oss} and C_{rss} varying with drain-source voltage V_{DS} are included in the datasheet, using WeEn's WNSC2M40120R as example. These capacitances display non-linear curves when plotted against V_{DS} and may be useful when considering gate drive losses, device parasitic turn-on and EMI behaviour.

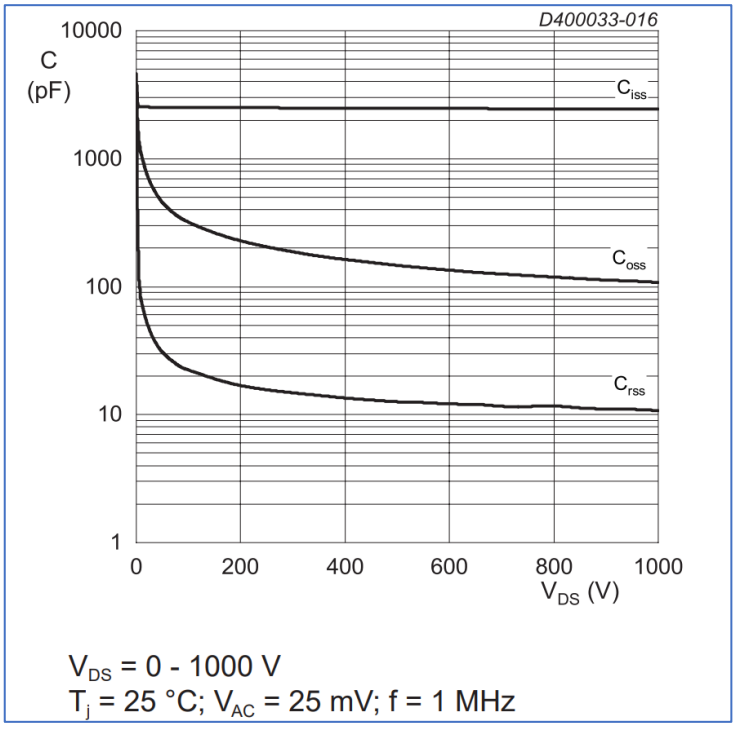


Fig.5. Example of capacitance characteristics VS drain source voltage.

Capacitance values are still included in datasheets and these three capacitances are normally as follows:

- **C_{iss}** (C_{iss} = C_{rss} + C_{GS})

This is the capacitance between the gate and the other two terminals (source and drain). The input capacitance is important in the design of the gate drive of the SiC MOSFET since this capacitance needs to be charged and discharged at every switching cycle and consequently decides the switching losses.

- **C_{oss}** (C_{oss} = C_{rss} + C_{DS})

This is the capacitance between the drain and the gate and source terminals. The output capacitance influences EMI behaviour because of its effect on the rate of change of V_{DS}, dV_{DS}/dt.

- **C_{rss}** (reverse transfer capacitance or "Miller" capacitance), $C_{rss} = C_{GD}$

This is the capacitance between the drain and the gate. This "Miller" capacitance determines the time-constant which relates to the crossing time between voltage and current at switching and so influences switching losses. A useful ratio is C_{GD}/C_{GS}, when high dv/dt is present during switching, the gate-source voltage is generated corresponding to the capacitance ratio of the parasitic capacitor C_{GD}/C_{GS}. At this time, if the gate-source voltage value exceeds Vth of SiC MOSFET, it will be mistakenly turned on, as shown in Fig7.

For WeEn's SiC MOSFET, the design value of C_{GD}/C_{GS} is low, this enables the device fast switching and suppresses mistakenly turned on.

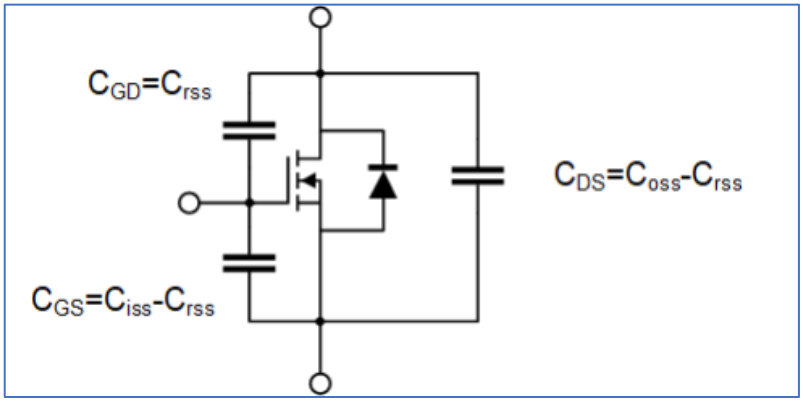


Fig. 6. Equivalent model of capacitance for SiC MOSFET

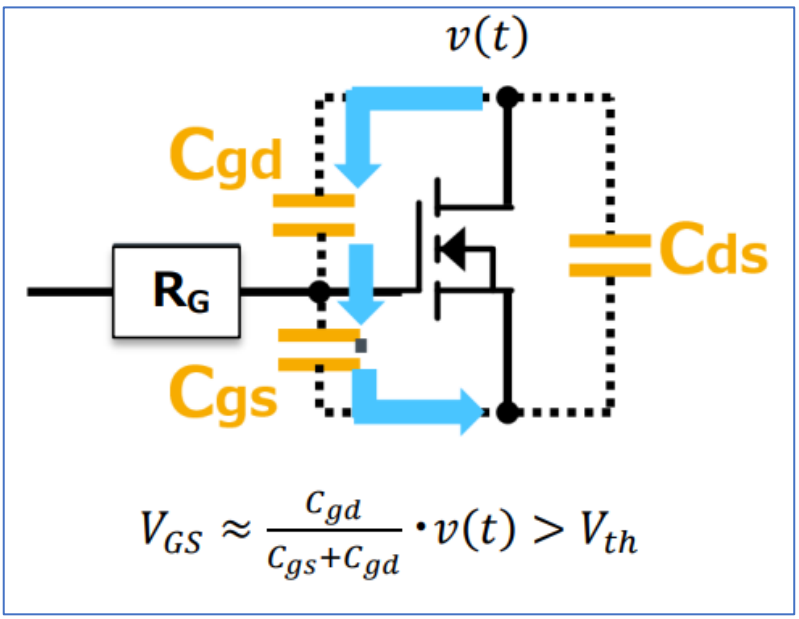


Fig. 7. Example of mistakenly turned on

3 Gate Driver Selection and Design Points

3.1 Drive Current

The driver chip generally charges and discharges the gate capacitor by using the source current and the sink current to make the SiC MOSFET switch on and off. To achieve lower switching losses and higher switching frequencies based on the fast-switching characteristics of SiC MOSFETs, it is necessary to select a driver chip with a large peak output current for SiC MOSFET. Fig. 8 shows the charging and discharging path of the driver circuit, using TI driver UCC53X0 as example.

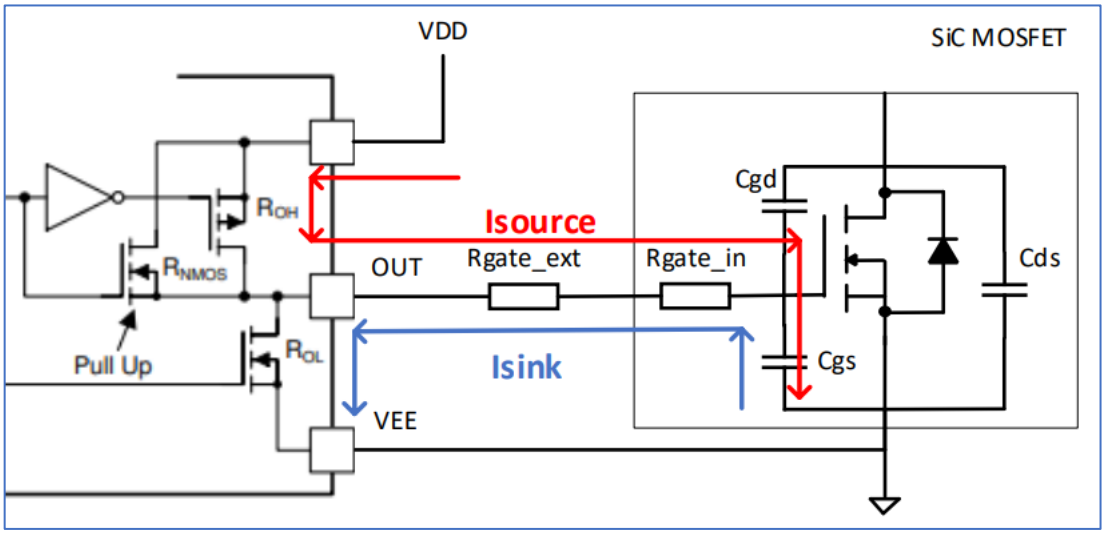


Fig. 8. example of the charging and discharging path

The driver's datasheet usually indicates the peak output source current and sink current, this also represents the saturation current of the internal Si MOSFET which design at the output stage in the driver chip. However, the maximum output current is generally related to the supply voltage, drive resistance and parasitic parameters of the drive loop in the actual system application. Fig. 9 shows the typical output source current and sink current, using TI driver and Infineon driver as example.

Device information

Product type	Typical output current and configuration
1ED3120MU12H	5.5 A separate source and sink
1ED3121MU12H	5.5 A separate source and sink
1ED3122MU12H	10.0 A and 3.0 A clamp
1ED3123MU12H	14.0 A separate source and sink
1ED3124MU12H	14.0 A separate source and sink
1ED3131MU12H	5.5 A separate source and sink, 180 ns minimum input pulse suppression time

DEVICE OPTION(1)	PACKAGE	MINIMUM SOURCE CURRENT	MINIMUM SINK CURRENT
UCC5310MC	D	2.4 A	1.1 A
	DWV		
UCC5320EC	D	2.4 A	2.2 A
UCC5320SC	D	2.4 A	2.2 A
	DWV		
UCC5350MC	D	5 A	5 A
	DWV		
UCC5350SB	D	5 A	5 A
UCC5390EC	D	10 A	10 A
	DWV		
UCC5390SC	D	10 A	10 A

Fig. 9. example of the typical output source and sink current

The peak output current is often limited by the impedance of the drive loop, which includes both the internal resistance ROL and ROH of the push-pull stage inside the driver chip, and the external drive resistance Rgate_ext and the internal gate resistance Rgate_in of the SiC MOSFET. The actual peak drive current calculation can see below formula:

$$I_{source} = \min\left(peak\ source, \frac{VDD}{R_{NMOS}||R_{OH} + R_{gate\_ext} + R_{gate\_in}}\right)$$

$$I_{sink} = \min\left(peak\ sink, \frac{VDD}{R_{OL} + R_{gate\_ext} + R_{gate\_in}}\right)$$

The data R_{OH}, R_{OL} and R_{NMOS} are usually given in the driver datasheet. Fig.10 shows related parameters, using TI driver UCC53X0 as example.

Table 8-1. UCC53x0 On-Resistance

DEVICE OPTION	R_{NMOS}	R_{OH}	R_{OL}
UCC5320SC and UCC5320EC	4.5	12	0.65
UCC5310MC	4.5	12	1.3
UCC5390SC and UCC5390EC	0.76	12	0.13
UCC5350MC	1.54	12	0.26
UCC5350SB	1.54	12	0.26

Fig. 10. example of related parameters

3.2 Drive Voltage

To improve the ease of use of SiC MOSFET in system application design, semiconductor manufacturers will try to adjust the compromise of parameters at the beginning of the design of SiC MOSFET. So that the driving characteristics of SiC MOSFET are close to silicon IGBT or silicon MOSFET which are familiar to users. But there are still many challenges to overcome, caused by un-mature technology and the process of SiC MOSFET. Therefore, it can be seen the difference Vgs range from different semiconductor manufacturers. The detailed value can be seen in table.1.

Therefore, the ideal driver chip for SiC MOSFETs should be able to cover a variety of different gate on and off voltage requirements, at least the driver chip's supply voltage differential from Vpos to Vneg can reach 25V. At least, the typical values of the Vpos and Vneg output supplies for bipolar operation can reach 20 V and –5 V for SiC MOSFETs.

Table. 1. example of Vgs value from semiconductor manufacturers

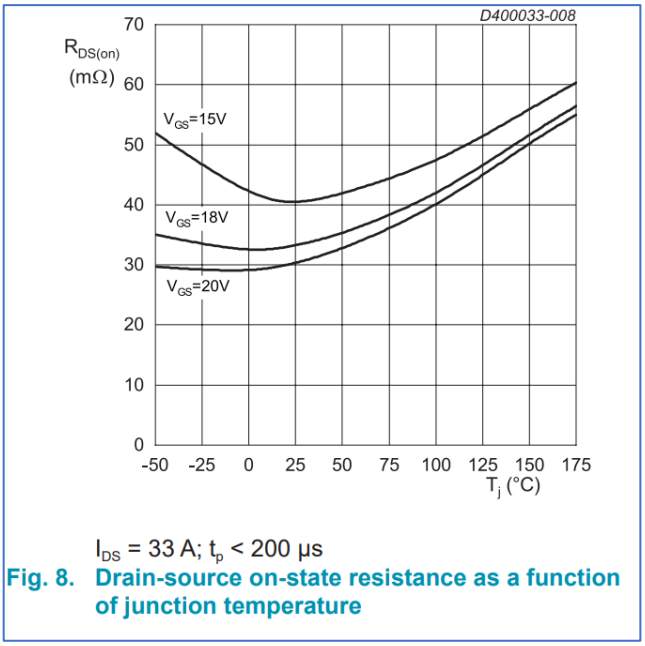
Manufacture	WeEn	Cree	Infineon	On semi	Rohm
Part Number	WNSC2M40120R	C3M0040120K	IMZA120R040M1H	NVH4L040N120M3S	SCT3040KR
Vgs,max	-12V & +24V	-8V & +19V	-7V & 20V	-10V & +22V	-4V & +22V
Vgs,op	-4V & +18V	-4V & +15V	-5V & +15V/+18V	-3V & +18V	0V & +18V

For WeEn's SiC MOSFET, it is generally recommended that gate source voltage use -4V & +18V in gate drive design. This is an optimization recommendation based on comprehensive consideration of performance and reliability, as shown in below formula:

$$+Vgs \uparrow \begin{cases} \nearrow E_{ON} \downarrow \\ \rightarrow E_{OFF} - \\ \searrow R_{DSon} \downarrow \end{cases} \rightarrow \begin{matrix} T_{sc} \downarrow \\ P_{driver} \uparrow \end{matrix}$$

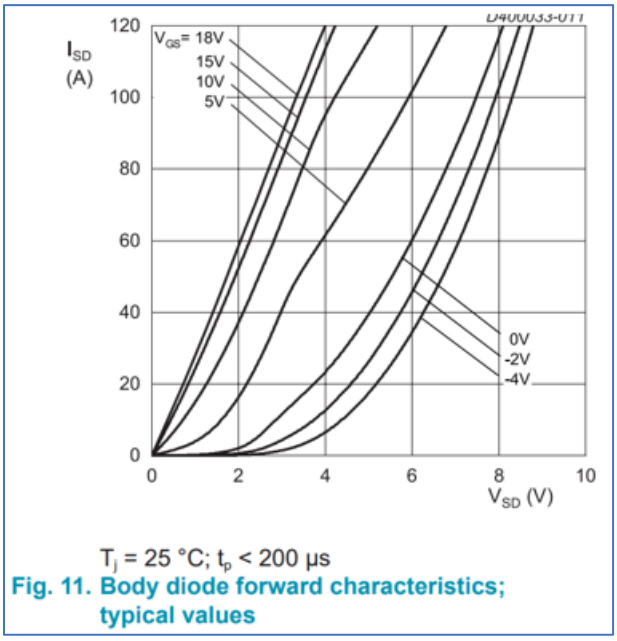
$$-Vgs \downarrow \begin{cases} \nearrow E_{OFF} \downarrow \\ \searrow E_{ON} - \end{cases} \rightarrow \begin{matrix} P_{driver} \uparrow \\ V_{SD} \uparrow \end{matrix}$$

With the increase of positive gate voltage bias, the on-resistance ($R_{DS(ON)}$) decreases, the on-switching loss (E_{ON}) also decreases, and the off-switching loss (E_{OFF}) does not change significantly, as shown in Fig.11 and table 2. But the increased voltage will lead to the decrease of short circuit time and the increase of the drive power, as shown in Fig.12. Higher gate drive voltage and inevitable voltage spikes will put more pressure on the gate oxide. So, the positive gate source voltage is recommended at +18V which can lead lower power losses and improve efficiency in system application.



I_{DS} = 33 A; t_p < 200 µs

Fig. 8. Drain-source on-state resistance as a function of junction temperature



T_j = 25 °C; t_p < 200 µs

Fig. 11. Body diode forward characteristics; typical values

Fig. 11. example of on state resistance vs positive gate voltage & body diode forward characteristics

Table. 2. example of switching losses test vs gate source voltage

Gate-Source Voltage (5Ω, 25℃)	Eon(μJ)	Eoff(μJ)
-5V – +20V	377	25
0V – +20V	414	38
-5V – +18V	467	25
0V – +18V	505	38

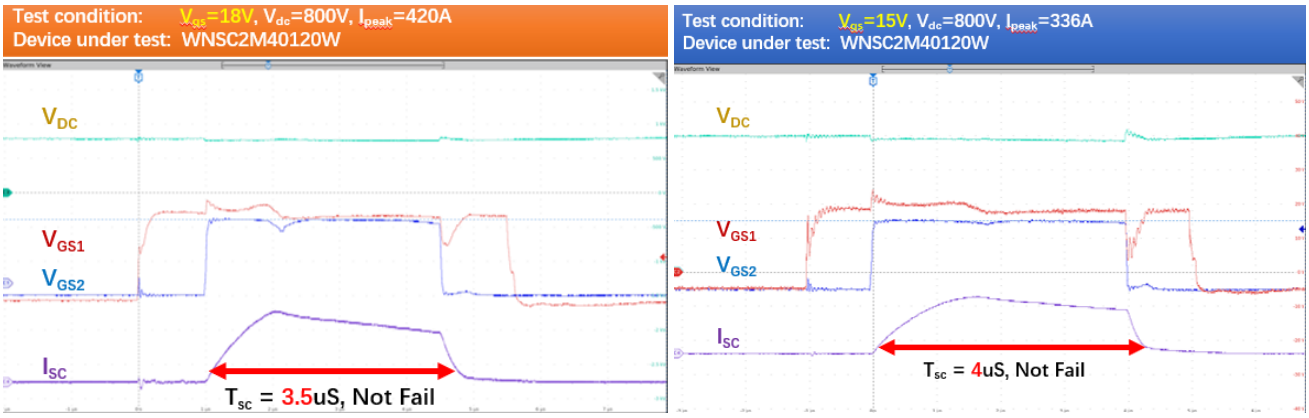


Fig. 12. example of short circuit test results

When the negative gate voltage bias increases to a negative value, the turn-off switch loss (E_{OFF}) decreases, and the on-switch loss (E_{ON}) does not change, as shown in table 2. But in the body diode, the forward voltage (V_F) increases, as shown in Fig.11. Due to unstable channel closure at VGS=0V and decreased channel current as negative bias increases. The reverse recovery feature will be slightly worse. Also, it will lead the increase of the drive power. Similarly, higher gate drive voltage and inevitable voltage spikes will put more pressure on the gate oxide. So, the negative gate source voltage is recommended at -4V which can lead lower power losses and more acceptable forward voltage of body diode in system application.

3.3 Gate resistance

The external gate-driver resistors, RG(ON) and RG(OFF) are used to:

1. Limit ringing caused by parasitic inductances and capacitances.
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery.
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss.

4. Reduce electromagnetic interference (EMI).

How to choose a suitable resistor is the key point in the driver design. There are some considerations as below:

The constraint conditions of turn on resistance are:

1. Adjust the turn on resistance, ensure that the reverse recovery voltage between body diode should be not exceeded the value of VDS, as shown in chapter 2.1. The test condition may be at system maximum operation voltage and maximum operation current or at system maximum operation voltage and 10%~20% operation current. Usually, the test temperature needs at low, room and high temperatures, as shown in Fig.13. It shows the spike voltage between SiC MOSFET and body diode is 840V in room temperature at left picture and the spike voltage between SiC MOSFET and body diode is 977V in high temperature at right picture at the same test conditions of voltage and current.

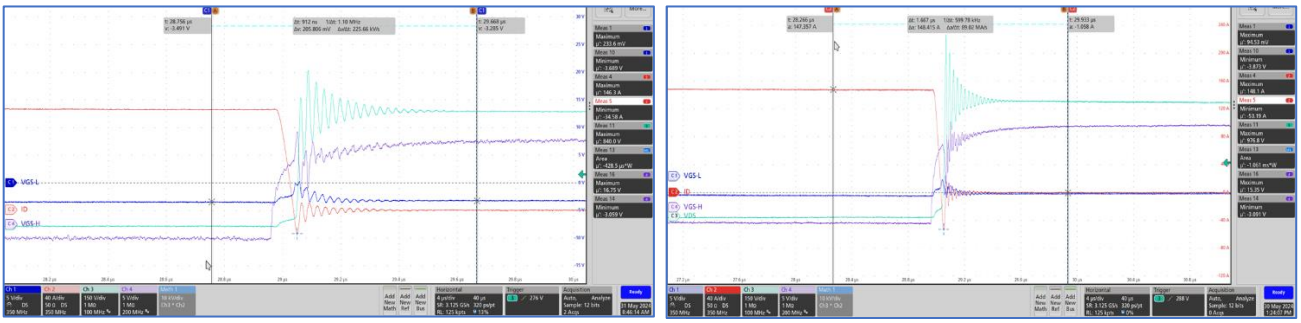


Fig. 13. example of reverse recovery test waveform

2. Adjust the turn on resistance, ensure that the complementary SIC MOS gate voltage should be not exceeding the minimum value of $V_{GS\,(th)}$, as shown in chapter 2.2. The test condition may be at system maximum operation voltage and maximum operation current or at system maximum operation voltage and 10%~20% operation current. Usually, the test temperature needs at low, room and high temperatures, as shown in Fig.14. It shows the spike voltage between gate and source is -0.06V in room temperature at left picture and spike voltage between gate and source is -0.1V in high temperature at right picture at the same test conditions of voltage and current.

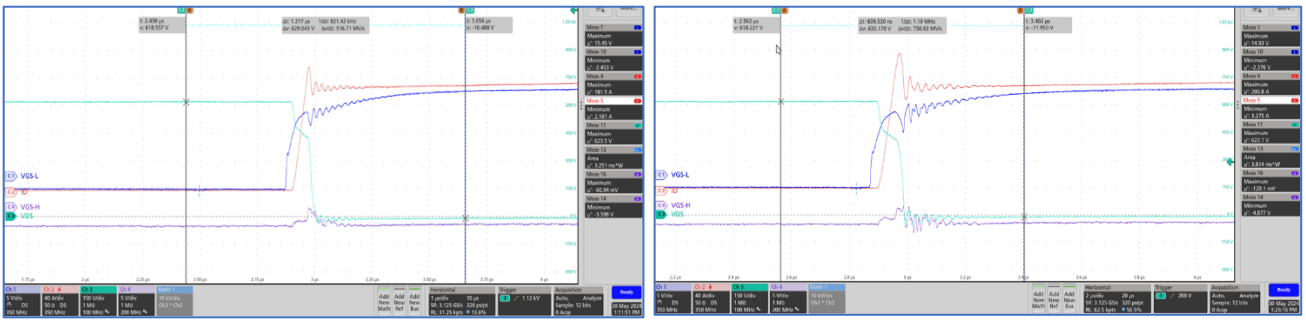


Fig. 14. example of turn on test waveform

3. Adjust the turn on resistance, ensure no significant sharply oscillation of the driving waveform at the position of the Miller platform. The test condition may be at system maximum operation voltage and maximum operation current or at system maximum operation voltage and 10%~20% operation current. Usually, the test temperature needs at low, room and high temperatures, as shown in Fig.15.

4. Reduce electromagnetic interference in system application.

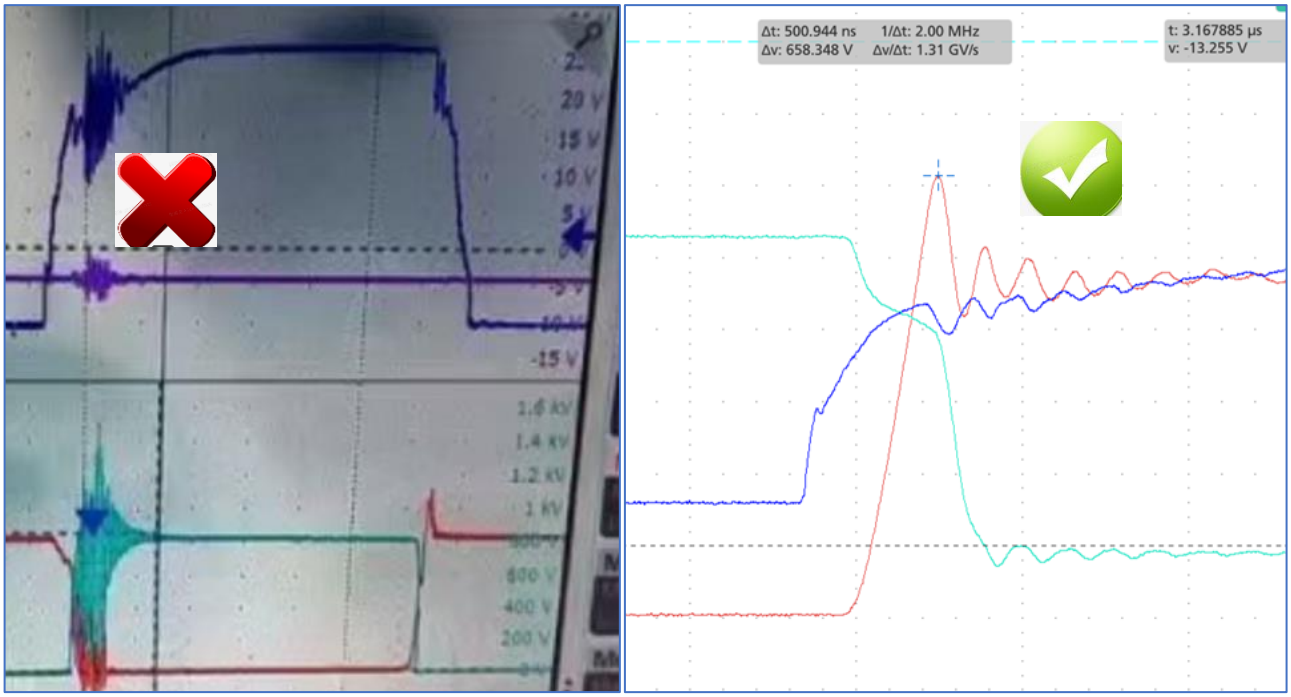


Fig. 15. example of turn on driving waveform

The constraint conditions of turn off resistance are:

1. Adjust the turn off resistance, ensure that the spike voltage between drain and source should be not exceeded the value of VDS, as shown in chapter 2.1. The test condition may be at system maximum operation voltage and maximum operation current. Usually, the test temperature needs at low, room and high temperatures, as shown in Fig.16. It shows the spike voltage between SiC MOSFET and body diode is 1047V in room temperature at left picture and the spike voltage between SiC MOSFET and body diode is 1006V in high temperature at right picture at the same test conditions of voltage and current.

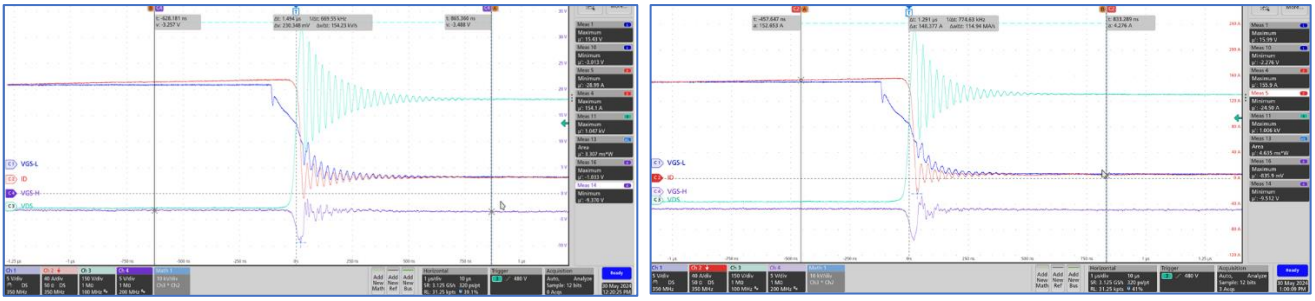


Fig. 16. example of turn off waveform

2. Adjust the turn on resistance, ensure that the complementary SIC MOS gate voltage should be not exceeding the maximum negative value of $V_{GS,max}$, as shown in chapter 2.1. The test condition may be at system maximum operation voltage and maximum operation current. Usually, the test temperature needs at low, room and high temperatures, as shown in Fig.16. It shows the spike voltage between gate and source is -9.4V in room temperature at left picture and spike voltage between gate and source is -9.5V in high temperature at right picture at the same test conditions of voltage and current.

3. Reduce electromagnetic interference in system application.

3.4 Active Miller Clamp

During MOSFET turning on, Cgd charged by gate current and discharged by miller current which generated by dv/dt. It remains the voltage of Vgs unchanged during this period. After Cgs reverse charge is completed, Vgs continues to rise to the driving voltage. The phenomenon of Vgs platform or shock during the on-off process is called Miller effect. SiC MOSFETs are usually used in high voltage and high frequency situations, which generates high dV/dt during the switching process. Using the half bridge circuit as an example, when the upper bridge is quickly opened and the lower bridge is closed, the Vds of the lower bridge will increase fast, and the charge will be transferred to the gate side of the lower bridge through the Miller capacitor Cgd. It will cause a small voltage spike on the gate when the current passes through R_G (R_G= R_{G_EXT} + R_{G_IN}), as shown in Fig. 17. If the voltage spike is higher than $V_{GS\ (th)}$, the SiC MOSFET will be turned on mistakenly, causing a serious short circuit problem.

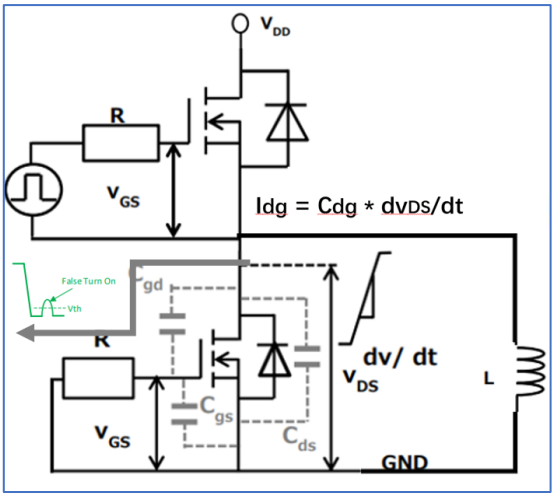


Fig. 17. example of SiC MOSFET turned on mistakenly by high dv/dt

To avoid the short circuit risk during the switching process, the driver voltage of SiC MOSFET usually use negative pressure. The negative pressure will make it lower than $V_{GS\ (th)}$ even there is a voltage spike occurs during the turn off process. But the excessive negative voltage spikes may break down them as the small negative pressure withstand capacity of SiC MOSFETs.

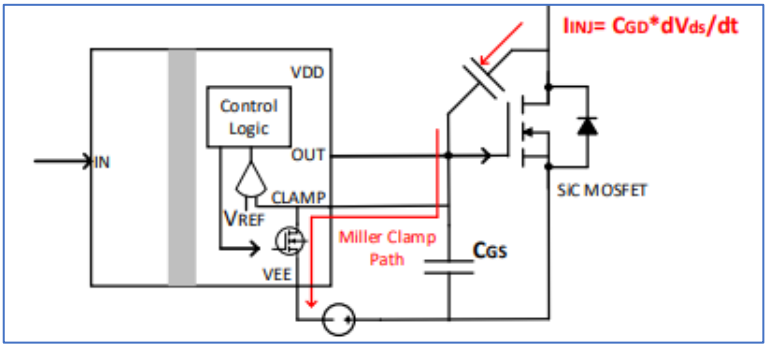


Fig. 18. example of active Miller Clamp function

The active Miller-clamp function helps to prevent a false turn-on of the power switches caused by Miller current in applications. The active Miller-clamp function is implemented by adding a low impedance path between the gate terminal and ground to bypass the miller current and prevent the high dV/dt introduced unintentional turn-on through the miller capacitance. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2 V during the off state. As shown is Fig18. Using Ti driver as example.

So, it is better to use active Miller clamp function in the design when SIC MOSFET has a high C_{GD}/C_{GS} and in the meantime high dv/dt in the application.

3.5 Short Circuit Protection

In many applications of power system, there are some over current and short circuit conditions. It not only requires the power device withstanding short circuit capacity, but also requires the gate driver to lock the device in a short corresponding time.

Figure 19 shows a common current detection circuit. The MOSFET source of the power loop is connected in series with a detection resistor Roc. When the current flows through the resistance Roc, a voltage Voc is generated. If the detected voltage is greater than the threshold voltage of the logic gate circuit, a short-circuit signal OC Fault is generated. At the same time the gate driver turns off the output.

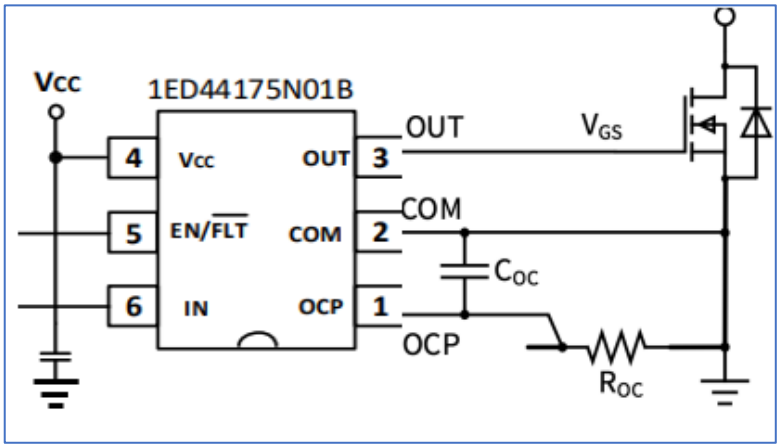


Fig. 19. Example of OCP driver design

The disadvantage of this circuit is that the resistance brings additional power loss. In the high-power system, the large current flowing through the detection resistance causes a large power loss. In low-power systems, larger resistance is needed to maintain the accuracy of the detection signal, which also affects the efficiency of the system.

Figure 20 shows a desaturation detection circuit. The method of desaturation detection is voltage detection. When the device implements a fast overcurrent or short-circuited, the voltage at both ends of the drain and source of the device will increase higher. It will trigger a desaturation fault in the gate driver.

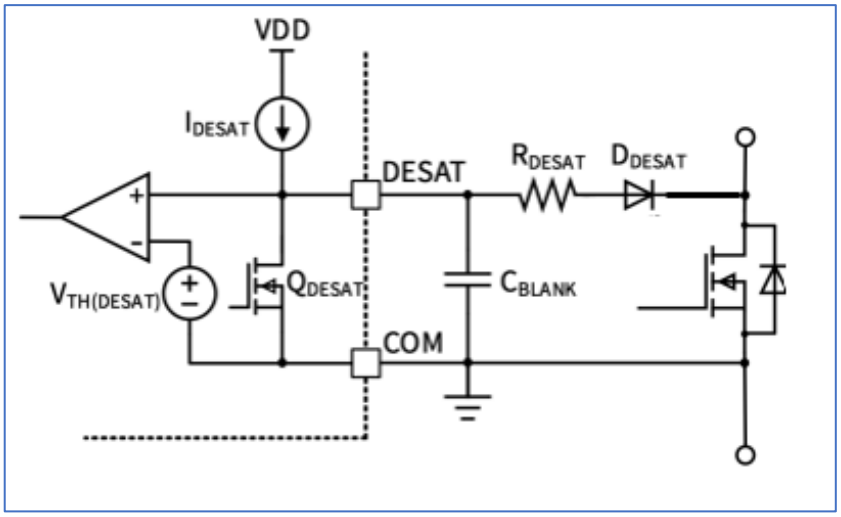


Fig. 20. Example of DESAT design

The DESAT pin of the device has a typical 9-V threshold with respect to COM, which connects the source of SIC MOSFET. When the input is in floating condition, or the output is held in low state, the DESAT pin is pulled down by an internal MOSFET and held in LOW state, which prevents the overcurrent and short circuit fault from false triggering. The internal current source of the DESAT pin is activated only during the driver ON state, which means the overcurrent and short circuit protection feature only works when the power semiconductor is in on state. The internal pulldown MOSFET helps to discharge the voltage of DESAT pin when the power semiconductor is turned off.

In the design of SiC MOS short circuit protection, it is necessary to consider both short circuit detection and short circuit shutdown. In the design of short circuit detection, the response speed and anti-interference performance should be considered. Short-circuit detection timely response, can avoid power module damage. The good anti-interference performance can avoid false triggering. Fig 21 shows a desaturation detection circuit in SIC MOSFET applications.

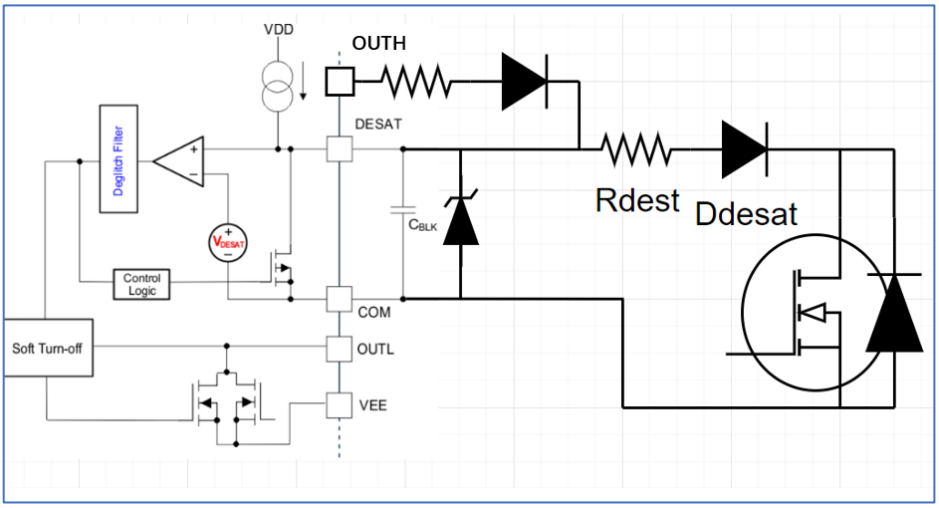


Fig. 21. Example of DESAT design in SIC MOSFET

3.6 Others

SiC The driver chip used by SiC MOSFET is in a high-frequency application environment, which requires the chip itself to have a high anti-interference degree. The parameter commonly used to evaluate the immunity of the driver chip is CMTI, and the CMTI of the driver chip needs to be greater than 150V/ns for high-frequency bridge circuit applications.

And other protection functions of gate drivers can be selected in the application design based on cost evaluation. Such as under voltage protection, over temperature protection, over voltage protection, watchdog, driver output check and two level turn off.

4 Typical Application

Figure 22 shows another example which uses two supplies. Power supply VA+ determines the positive drive output voltage and VA– determines the negative turn-off voltage. The power supply for high side and low side drivers also needs to be isolated. This solution requires more power supplies. However, it provides more flexibility when setting the positive and negative rail voltages.

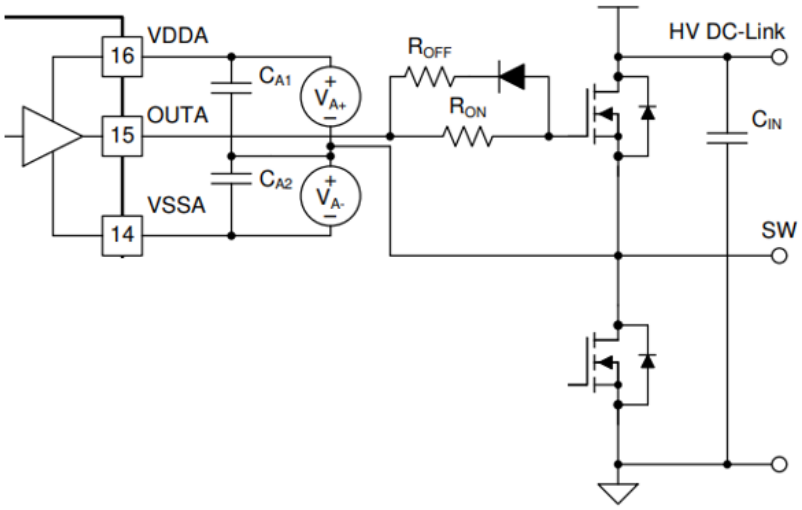


Fig. 22. Example of gate driver design with two supplies

Figure 23 shows the first example with negative bias turn-off on the driver using a Zener diode on the isolated power supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply, VA, is equal to 17 V, the turn-off voltage will be –5.1 V and turn-on voltage will be 17 V – 5.1 V ≈ 12 V. needs to be isolated. This configuration needs two isolated power supplies for a half-bridge configuration, and there will be steady state power consumption from RZ.

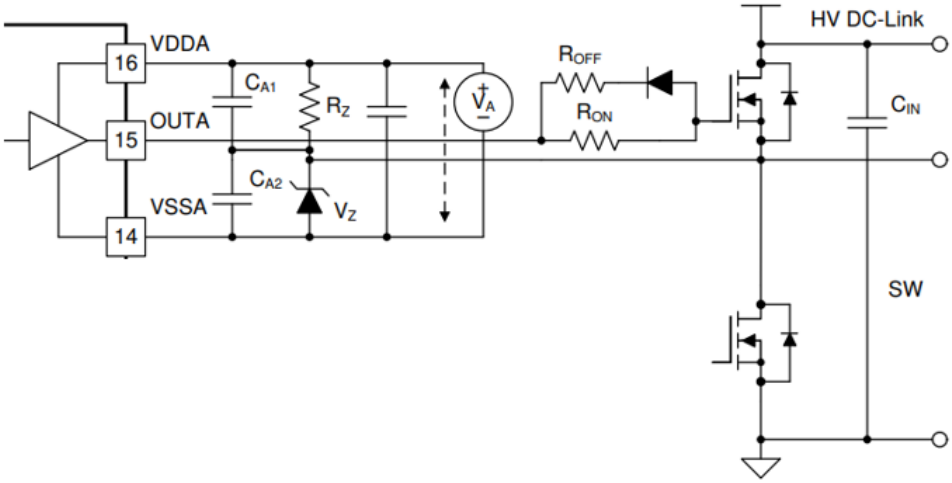


Fig. 23. Example of gate driver design with Zener diode

Figure 24 shows a single power supply configuration and generates negative bias through a Zener diode in the gate drive loop. The benefit of this solution is that it only uses one power supply, and the bootstrap power supply can be used for the high side drive. This design requires the least cost and design effort among the three solutions. However, the negative gate drive bias is not only determined by the Zener diode, but also by the duty cycle, which means the negative bias voltage will change when the duty cycle changes. Therefore, converters with a fixed duty cycle (~50%) such as variable frequency resonant convertors or phase shift convertors will favour this solution.

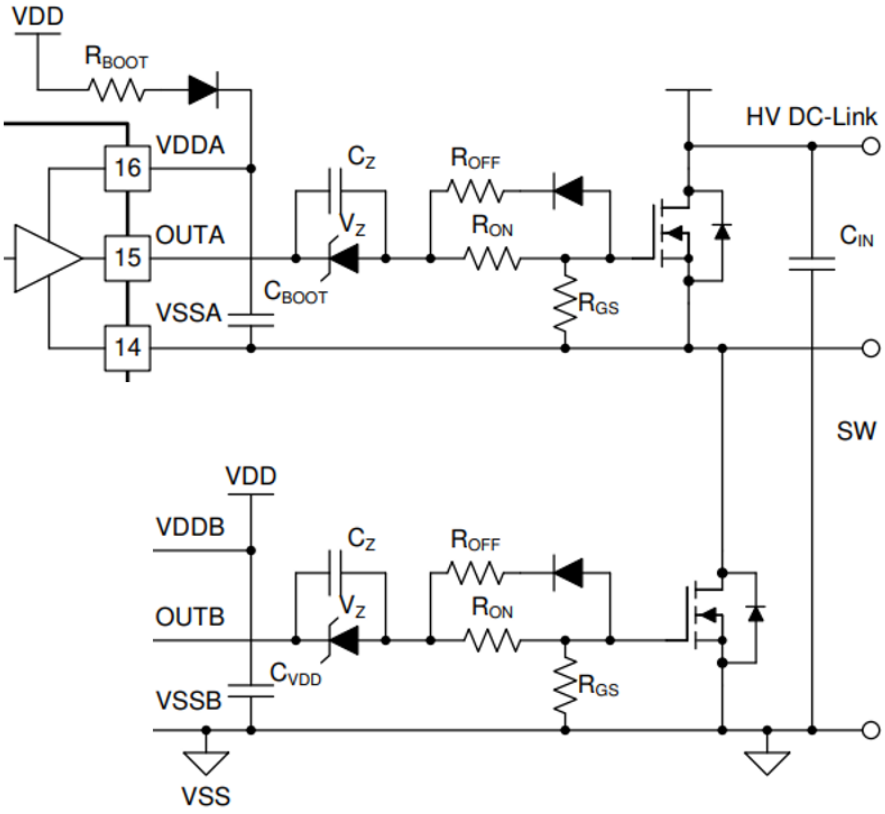


Fig. 24. Example of gate driver design with single power supply

1 Revision history

Rev	Date	Description
V.01	20241114	Initial version

2 Contact information

For more information and sales office addresses please visit: **http://www.ween-semi.com**

3 Contents

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