

1. General description

Planar passivated very sensitive gate four quadrant triac in a TO92 plastic package intended for use in applications requiring enhanced noise immunity and direct interfacing to logic ICs and low power gate drivers.

2. Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

4. Quick reference data

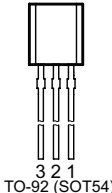
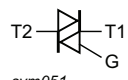
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Absolute maximum rating						
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 45\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(initial)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	12.5	A
		full sine wave; $T_{j(initial)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	13.8	A
T_j	junction temperature		-	-	125	°C
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	0.3	-	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	0.3	-	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	0.3	-	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7	0.3	-	7	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	-	10	mA
V_T	on-state voltage	$I_T = 1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.3	1.6	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536 \text{ V}$; $T_j = 110 \text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	100	-	-	V/ μs
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400 \text{ V}$; $T_j = 110 \text{ }^\circ\text{C}$; $di_{com}/dt = 0.44 \text{ A/ms}$; gate open circuit	1	-	-	V/ μs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2	 <p>TO-92 (SOT54)</p>	 <p>sym051</p>
2	G	gate		
3	T1	main terminal 1		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
Z0107NA0	TO92	Z0107NA0,412	Bulk	1000	SOT54	14-Nov-2013
Z0107NA0	TO92	Z0107NA0QP	Reel	2000	SOT54 wide pitch	14-Nov-2013
Z0107NA0/L02	TO92	Z0107NA0/L02EP	Bulk	500	SOT54	14-Nov-2013

7. Marking

Table 4. Marking codes

Type number	Marking codes
Z0107NA0	107NA0

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{lead} \leq 45\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	1	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	12.5	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	13.8	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	0.78	A ² s
di_T/dt	rate of rise of on-state current	$I_G = 20\text{ mA}$; T2+ G+	-	50	A/ μ s
		$I_G = 20\text{ mA}$; T2+ G-	-	50	A/ μ s
		$I_G = 20\text{ mA}$; T2- G-	-	50	A/ μ s
		$I_G = 20\text{ mA}$; T2- G+	-	20	A/ μ s
I_{GM}	peak gate current		-	1	A
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	125	°C

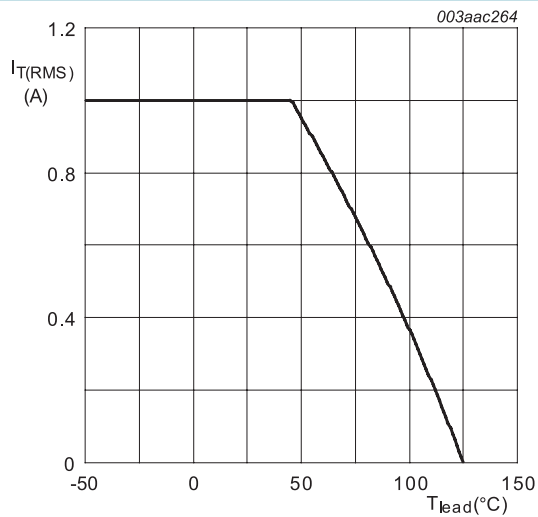
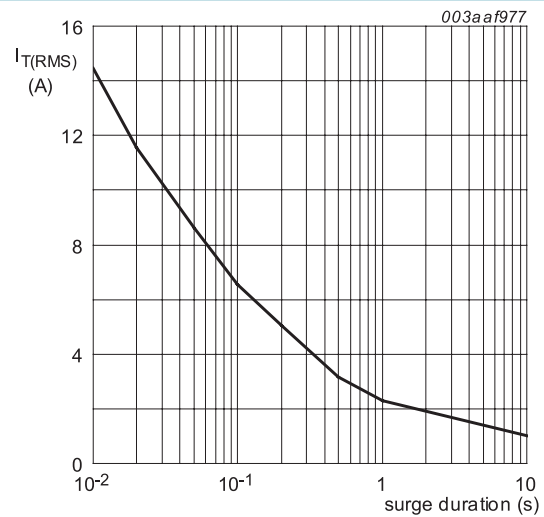
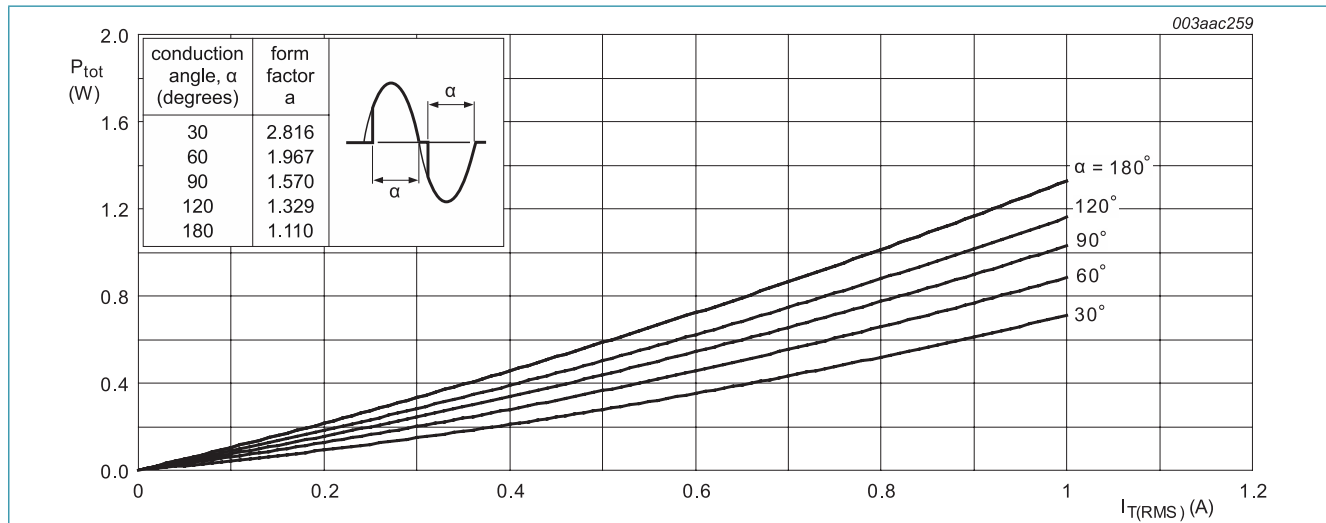


Fig. 1. RMS on-state current as a function of lead temperature; maximum values

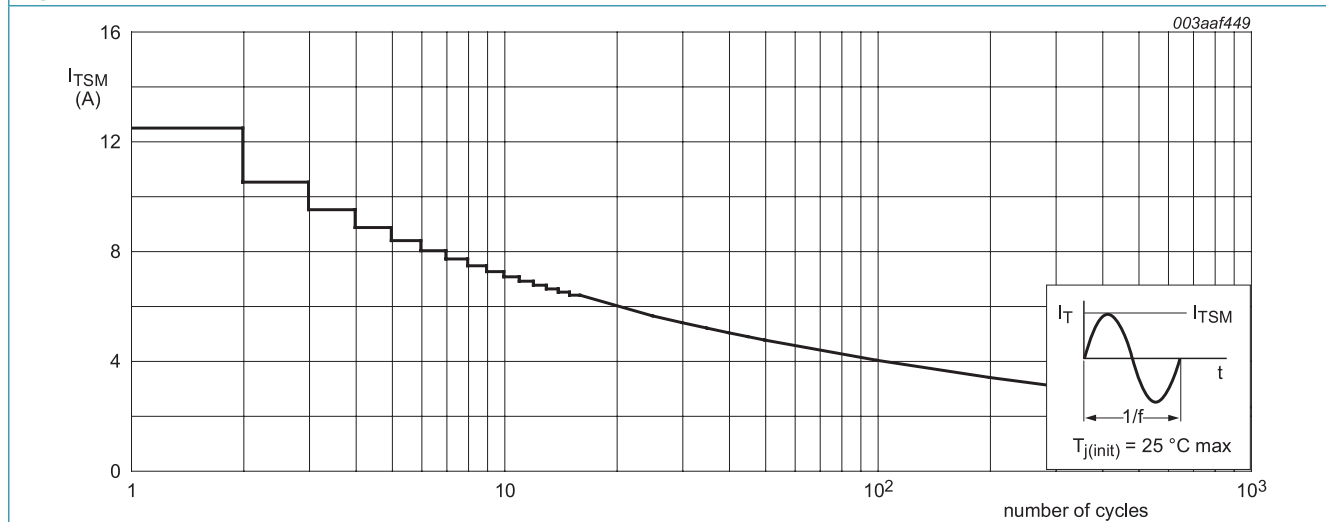


$f = 50\text{ Hz}$; $T_{lead} = 45\text{ °C}$
Fig. 2. RMS on-state current as a function of surge duration; maximum values



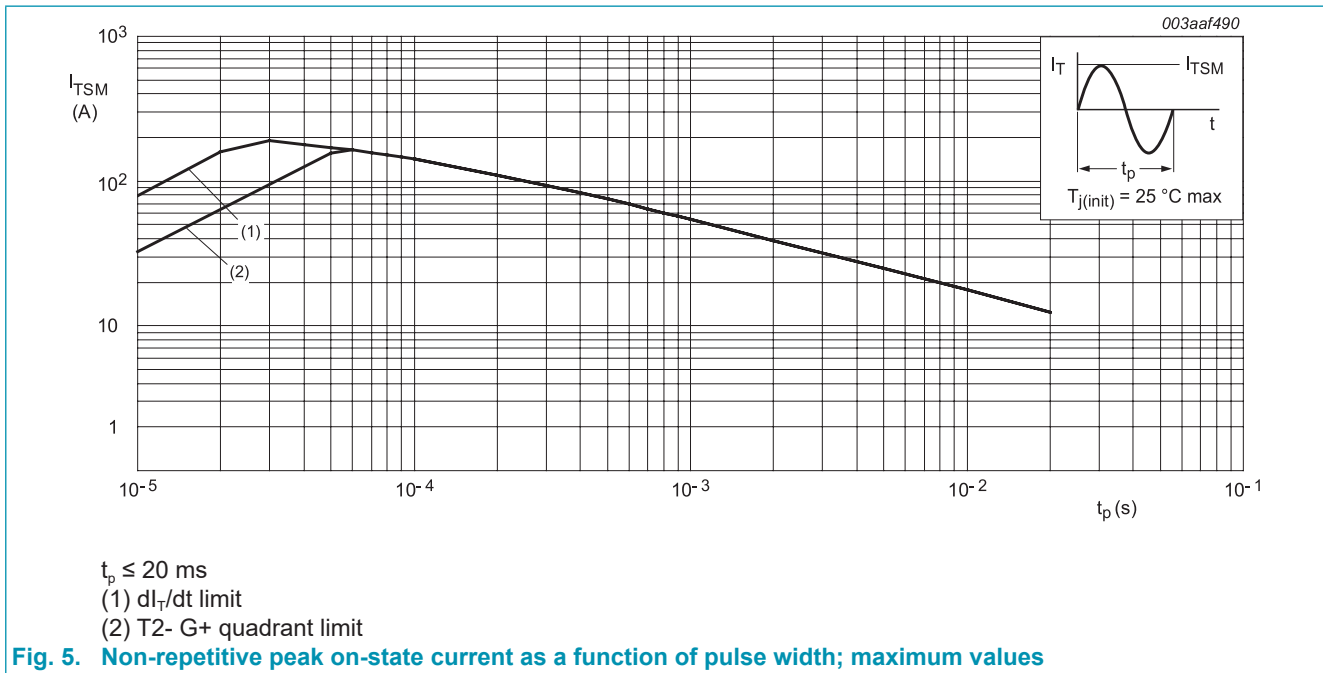
α = conduction angle
 a = form factor = $I_{T(RMS)} / I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



$f = 50\text{ Hz}$

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	full cycle; printed circuit board: lead length = 4 mm	-	150	-	K/W

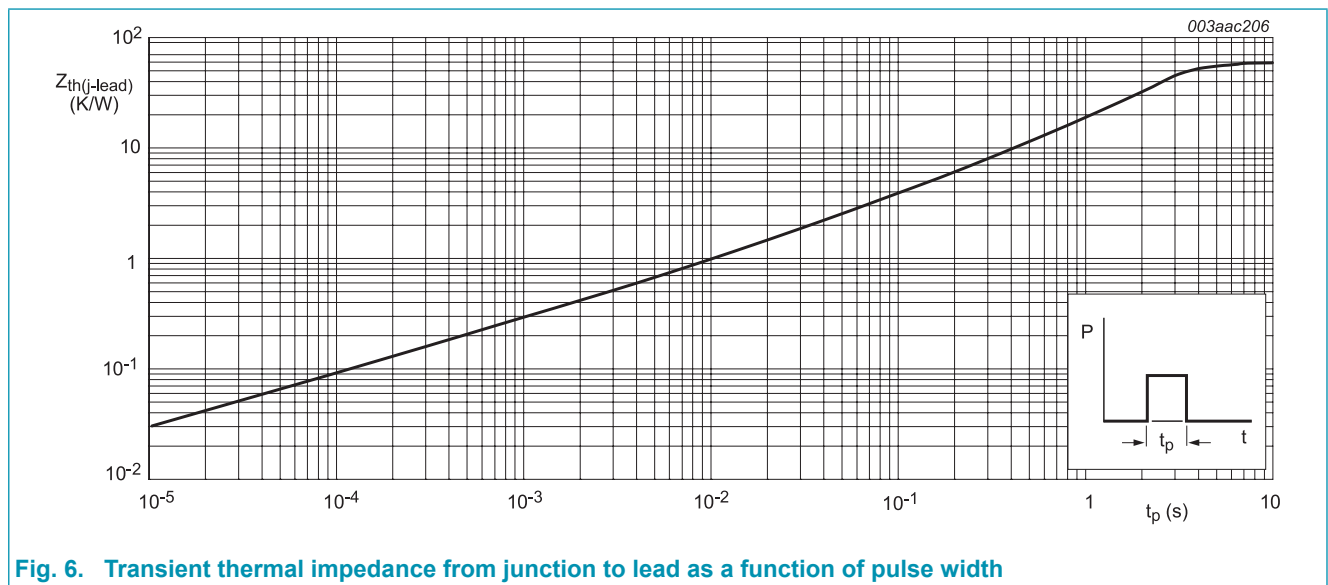


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 7	0.3	-	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 7	0.3	-	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 7	0.3	-	5	mA
		$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 7	0.3	-	7	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	10	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2+ G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	25	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	10	mA
		$V_D = 12\text{ V}$; $I_G = 0.1\text{ A}$; T2- G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	10	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	-	10	mA
V_T	on-state voltage	$I_T = 1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	1.3	1.6	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	-	1	V
		$V_D = 800\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 125\text{ °C}$	0.2	-	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 125\text{ °C}$	-	-	0.5	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 110\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	100	-	-	V/ μ s
dV_{com}/dt	rate of change of commutating voltage	$V_D = 400\text{ V}$; $T_j = 110\text{ °C}$; $dI_{com}/dt = 0.44\text{ A/ms}$; gate open circuit	1	-	-	V/ μ s

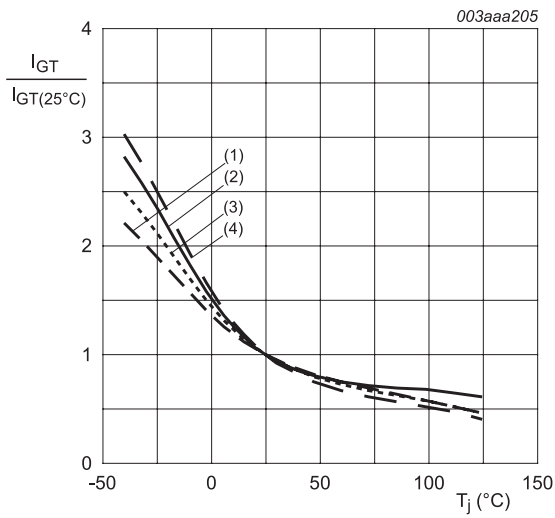


Fig. 7. Normalized gate trigger current as a function of junction temperature

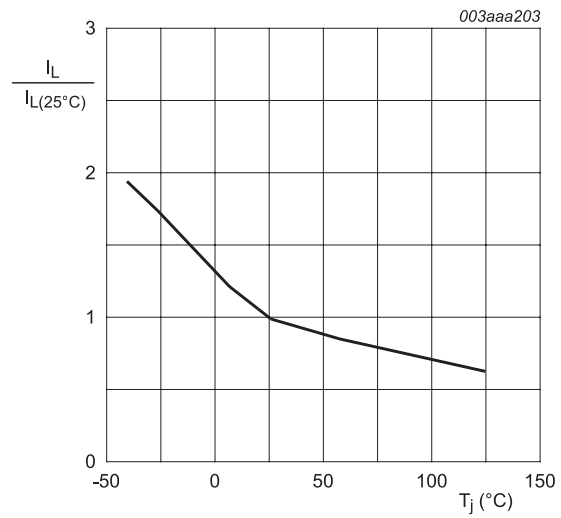


Fig. 8. Normalized latching current as a function of junction temperature

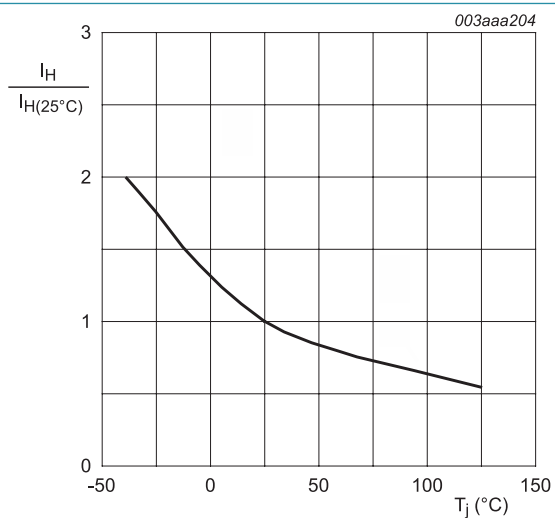
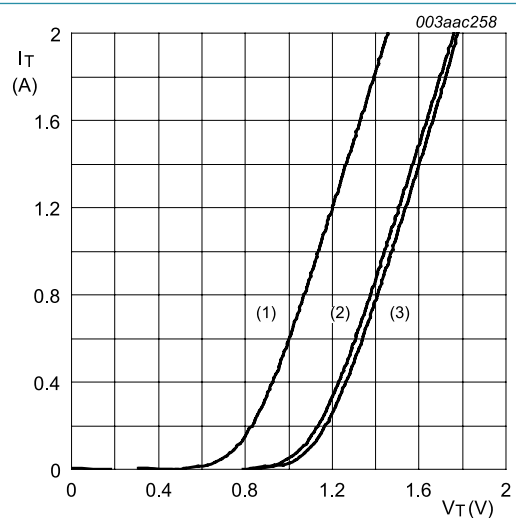


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.13\text{ V}; R_s = 0.31\ \Omega$
 (1) $T_j = 125^\circ\text{C}$; typical values
 (2) $T_j = 125^\circ\text{C}$; maximum values
 (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

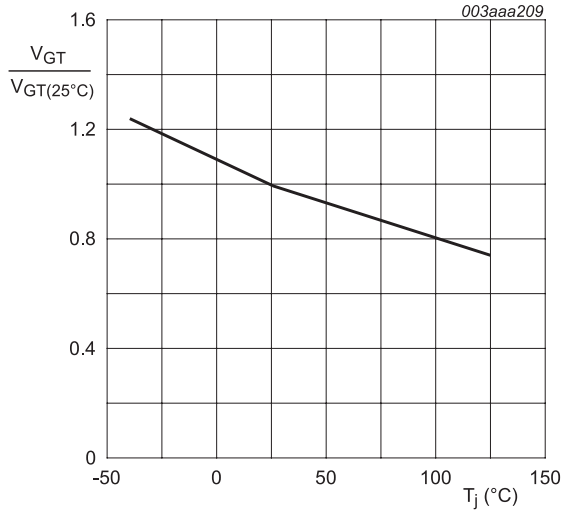
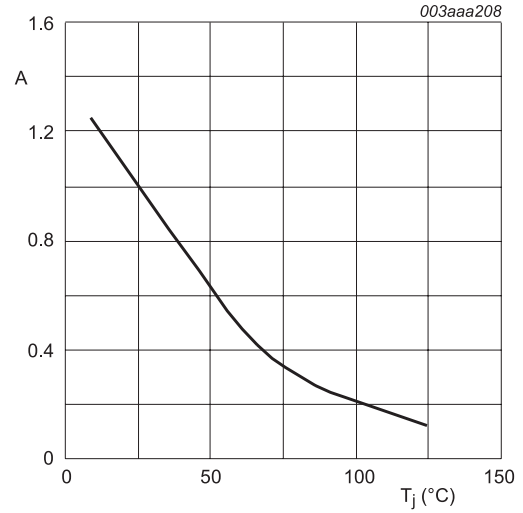


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

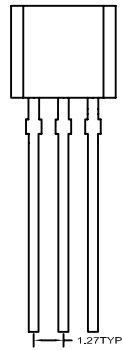


$$A = \frac{dV_D(T_j \text{ } ^\circ\text{C})/dt}{dV_D(25^\circ\text{C})/dt}$$

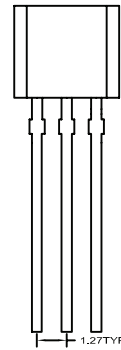
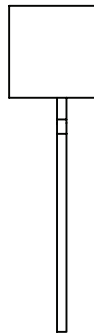
Fig. 12. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values

11. Package outline

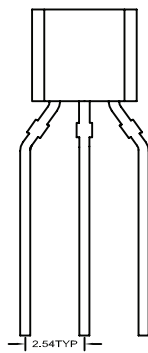
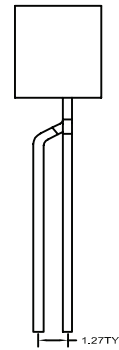
SOT54 PACKAGE OUTLINE



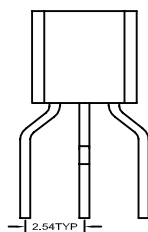
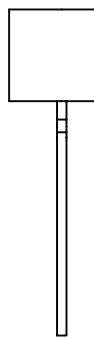
SOT54
Bulk Pack - 412



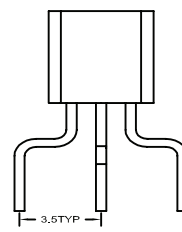
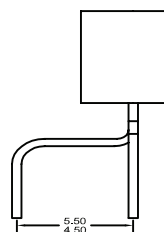
SOT54 LEADS ON CIRCLE
Bulk Pack - 112



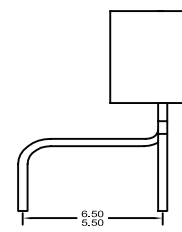
SOT54 WIDE PITCH
Tape/ Reel Pack - 116
Ammo Pack - 126



SOT54 LEAD BEND L01
Bulk Pack - 412



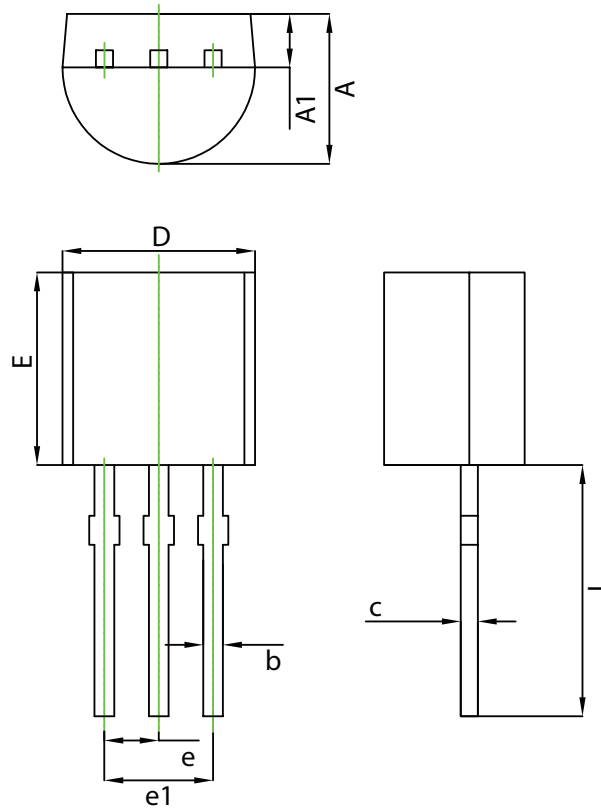
SOT54 LEAD BEND L02
Bulk Pack - 412



Remark: Detailed dimensions refer to POD drawing.

Plastic single-ended leaded(through hole) package; 3 leads

TO92



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.300	3.700	0.130	0.146
A1	1.100	1.400	0.043	0.055
b	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	4.300	4.700	0.169	0.185
E	4.300	4.700	0.169	0.185
e	1.270 TYP.		0.050 TYP.	
e1	2.440	2.640	0.096	0.104
L	14.100	14.500	0.555	0.571

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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For more information, please visit: <http://www.ween-semi.com>

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