

## 1. General description

Passivated, sensitive gate thyristors in a plastic envelope, intended for use in general purpose switching and phase control applications. These devices are intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- High blocking voltage suitable for high voltage applications
- Sensitive gate suitable for logic level controls

## 3. Applications

- General purpose switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	75	A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$	-	-	82	A
$T_j$	junction temperature		[1]	-	125	°C
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 7</a>	-	50	200	μA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ °C}$ ; $R_{GK} = 100\text{ }\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; <a href="#">Fig. 12</a>	50	100	-	V/μs

[1] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

## 6. Ordering information

Table 3. Ordering information

Type number	Package name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BT258-800R	TO220	BT258-800R,127	Tube	50	SOT78	13-Jun-2008

## 7. Marking

Table 4. Marking codes

Type number	Marking codes	
	Assembly factory: d	Assembly factory: A
BT258-800R	BT258 800R PJdxxxx xx	BT258 800R PJAxxxx xx

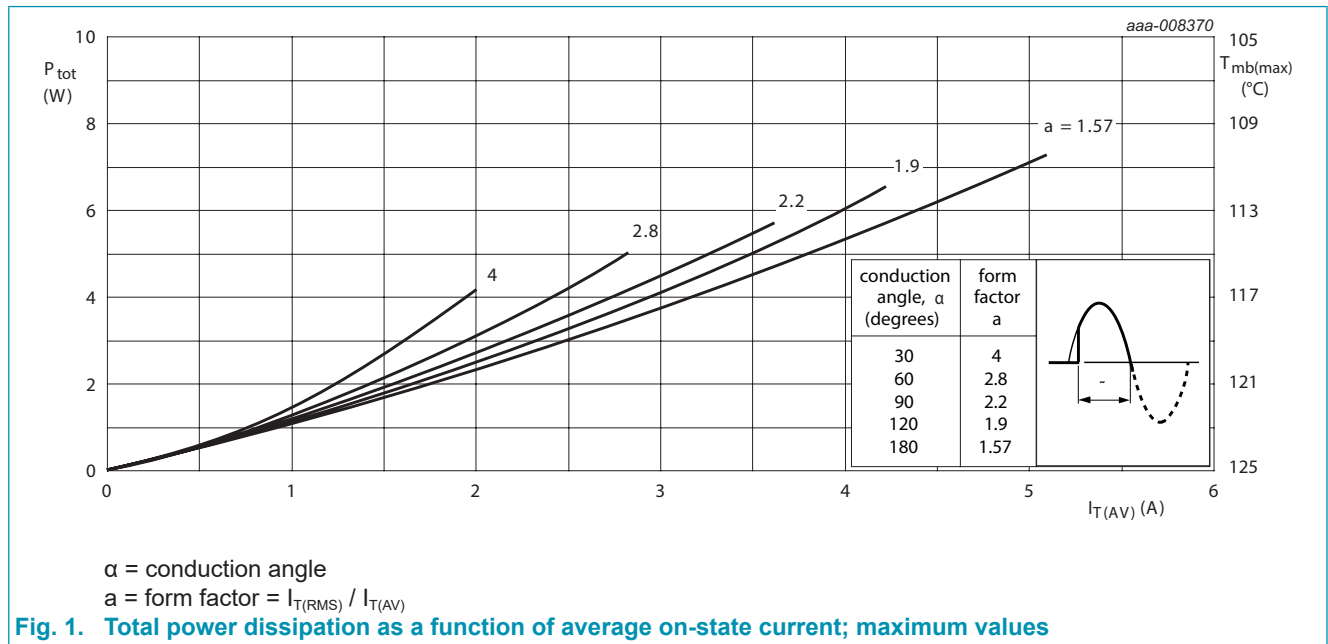
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	800	V
$V_{RRM}$	repetitive peak reverse voltage		-	800	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 1</a>	-	5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 111\text{ °C}$ ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	8	A
$I_{TSM}$	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 10\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	75	A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 8.3\text{ ms}$	-	82	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	28	$A^2s$
$di_T/dt$	rate of rise of on-state current	$I_T = 10\text{ A}$ ; $I_G = 50\text{ mA}$ ; $di_G/dt = 50\text{ mA}/\mu s$	-	50	$A/\mu s$
$I_{GM}$	peak gate current		-	2	A
$V_{RGM}$	peak reverse gate voltage		-	5	V
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}C$
$T_j$	junction temperature		[1]	125	$^{\circ}C$

[1] Operation above 110°C may require the use of a gate to cathode resistor of 1kΩ or less.



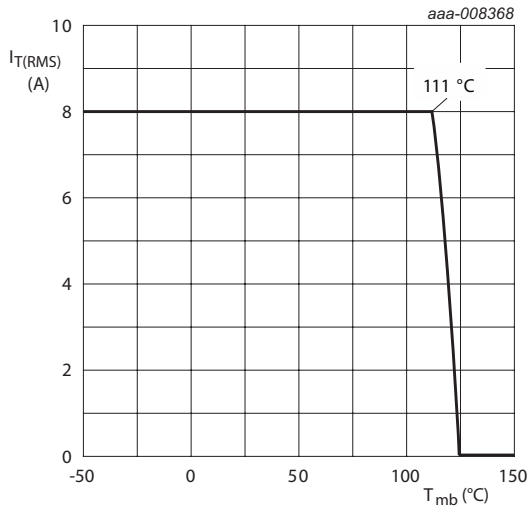


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values

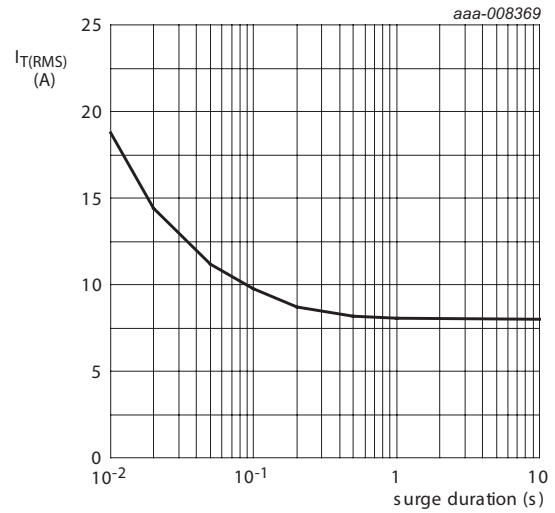


Fig. 3. RMS on-state current as a function of surge duration; maximum values  
 $f = 50 \text{ Hz}; T_{mb} = 111 \text{ °C}$

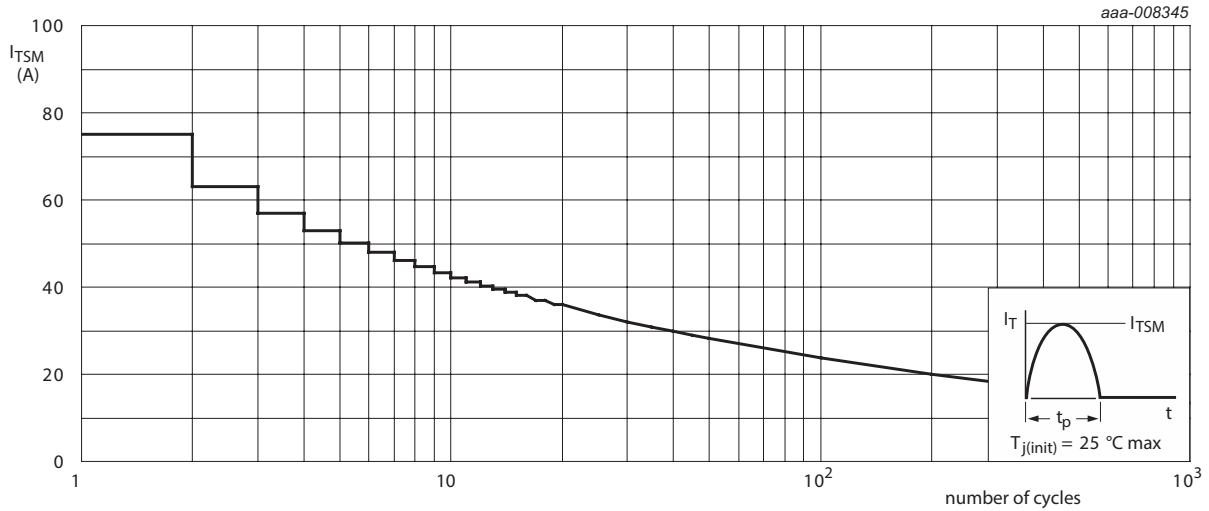
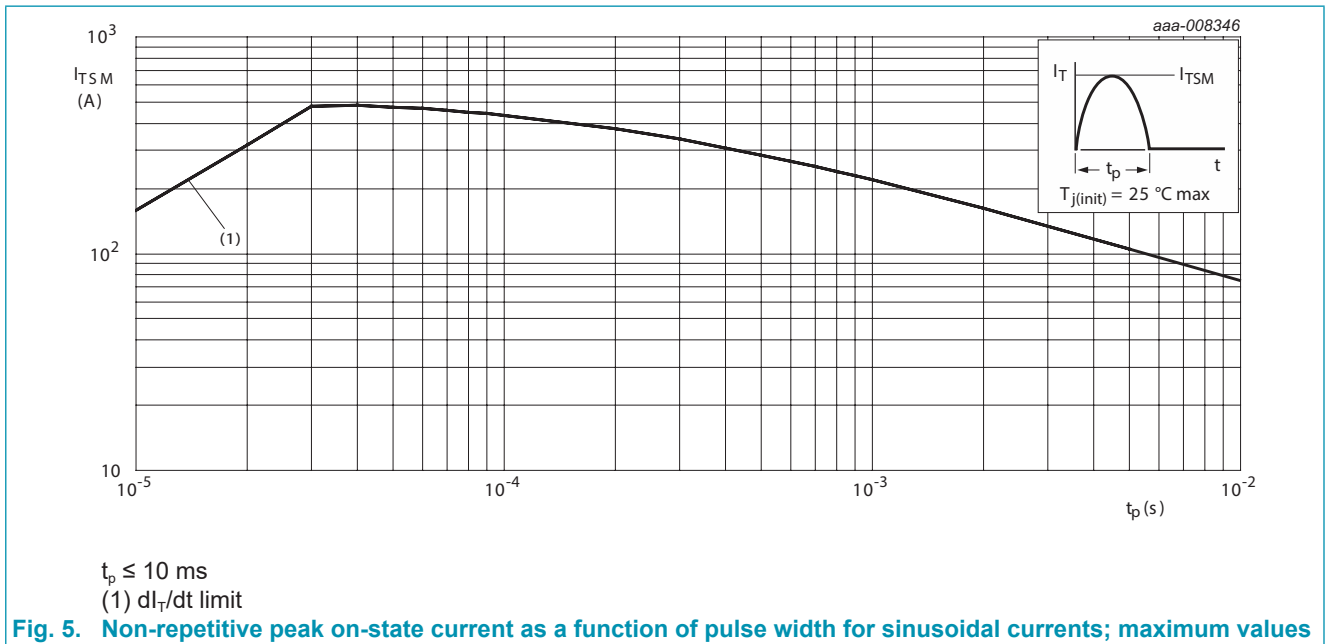


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values  
 $f = 50 \text{ Hz}$



## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 6</a>	-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	60	-	K/W

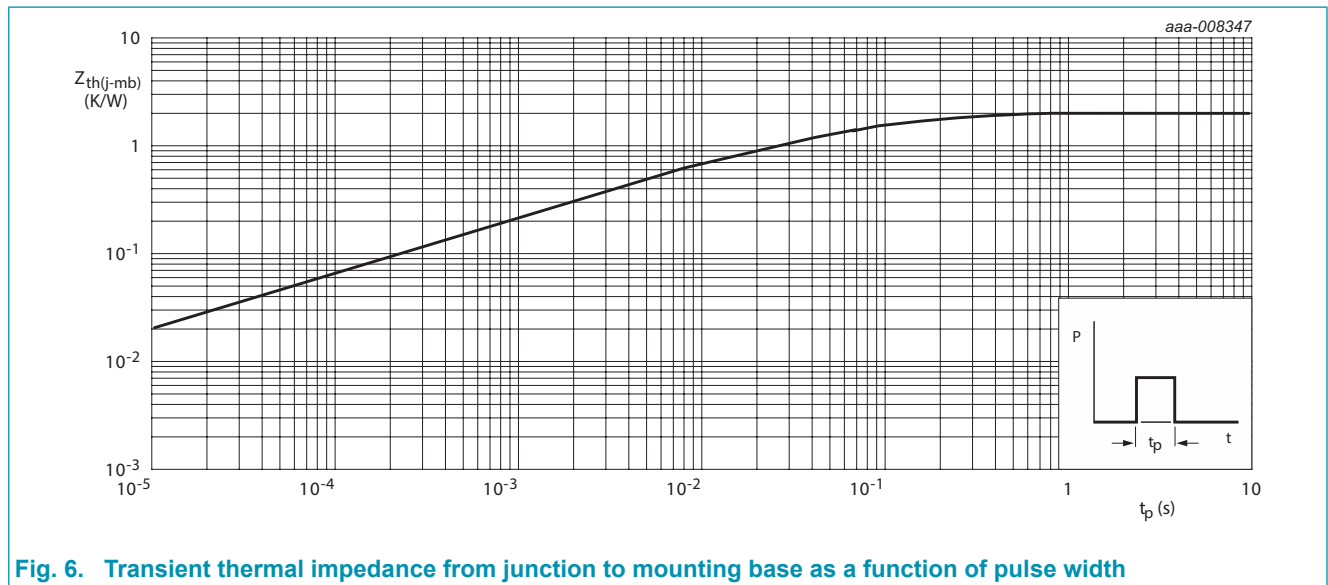
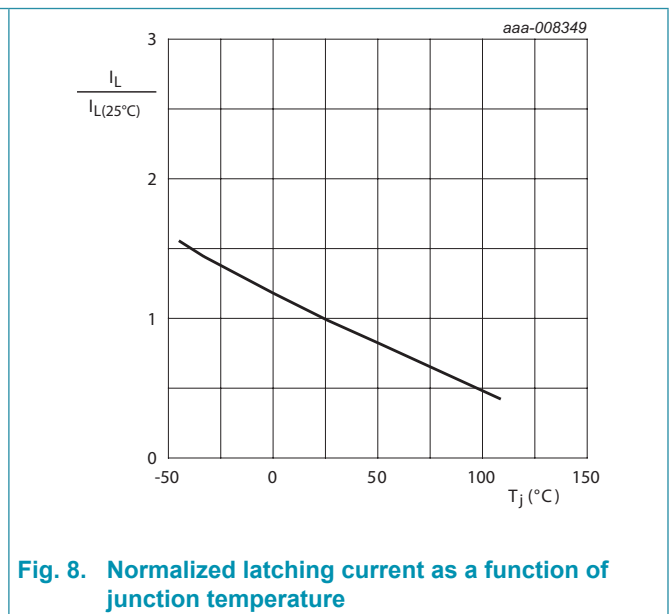
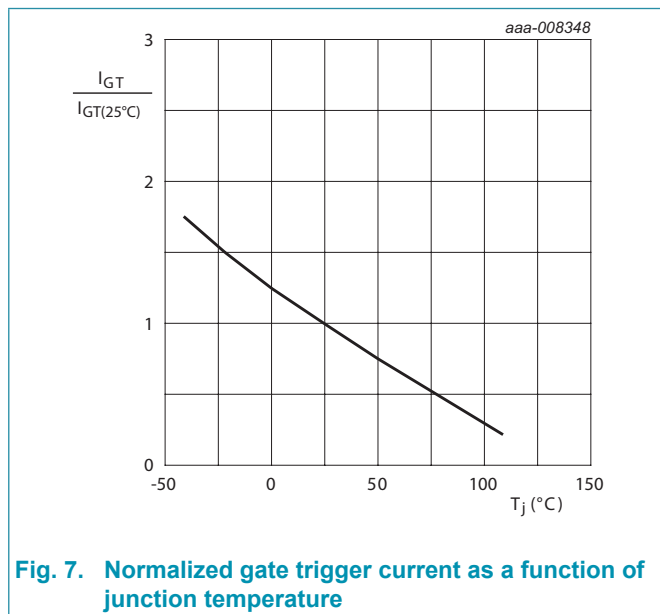


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

### 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 7	-	50	200	$\mu\text{A}$
$I_L$	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 8	-	0.4	10	mA
$I_H$	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 9	-	0.4	6	mA
$V_T$	on-state voltage	$I_T = 16\text{ A}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 10	-	1.3	1.6	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$ ; Fig. 11	-	0.4	1	V
		$V_D = 800\text{ V}; I_T = 0.1\text{ A}; T_j = 110\text{ }^\circ\text{C}$	0.1	0.2	-	V
$I_D$	off-state current	$V_D = 800\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
$I_R$	reverse current	$V_R = 800\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_j = 125\text{ }^\circ\text{C}; R_{GK} = 100\text{ }\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; Fig. 12	50	100	-	$\text{V}/\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 10\text{ A}; V_D = 800\text{ V}; I_G = 5\text{ mA}$ ; $dI_G/dt = 0.2\text{ A}/\mu\text{s}; T_j = 25\text{ }^\circ\text{C}$	-	2	-	$\mu\text{s}$
$t_q$	commutated turn-off time	$V_{DM} = 536\text{ V}; T_j = 125\text{ }^\circ\text{C}; I_{TM} = 12\text{ A}; V_R = 24\text{ V}$ ; ( $dI_T/dt$ ) <sub>M</sub> = 10 A/ $\mu\text{s}$ ; $dV_D/dt = 2\text{ V}/\mu\text{s}$ ; $R_{GK(ext)} = 1\text{ k}\Omega$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ )	-	100	-	$\mu\text{s}$



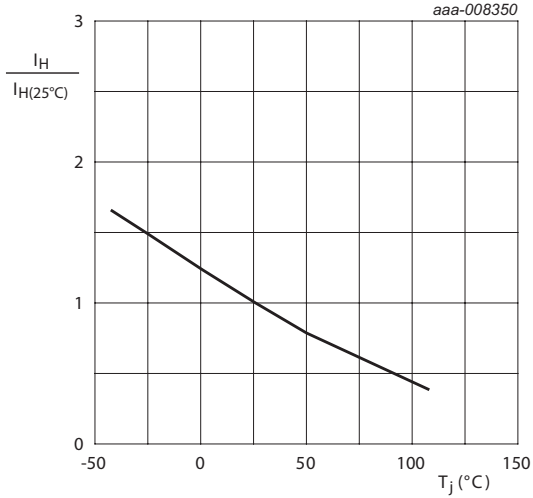
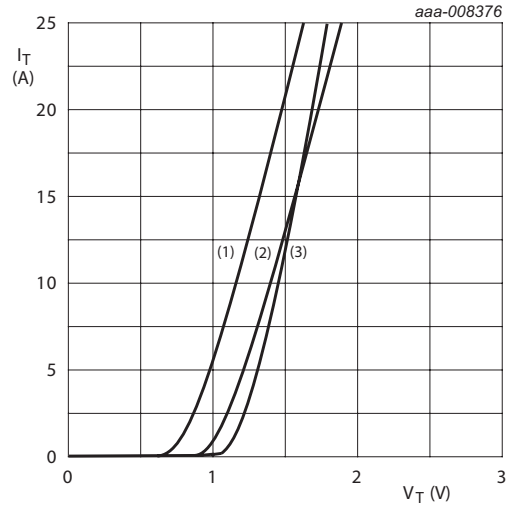


Fig. 9. Normalized holding current as a function of junction temperature



$V_0 = 1.0 \text{ V}; R_s = 0.04 \ \Omega$   
 (1)  $T_j = 125 \text{ }^\circ\text{C}$ ; typical values  
 (2)  $T_j = 125 \text{ }^\circ\text{C}$ ; maximum values  
 (3)  $T_j = 25 \text{ }^\circ\text{C}$ ; maximum values

Fig. 10. On-state current as a function of on-state voltage

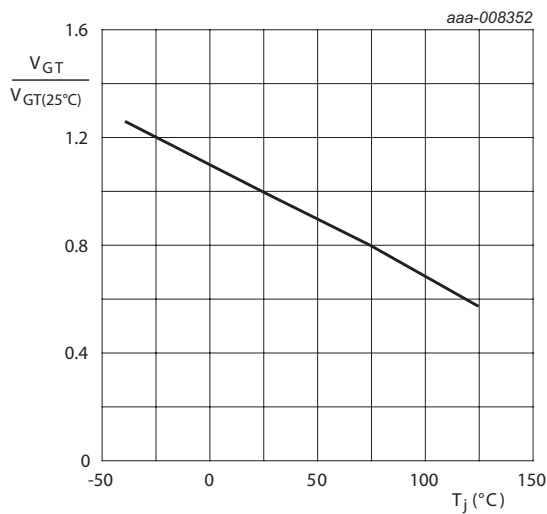
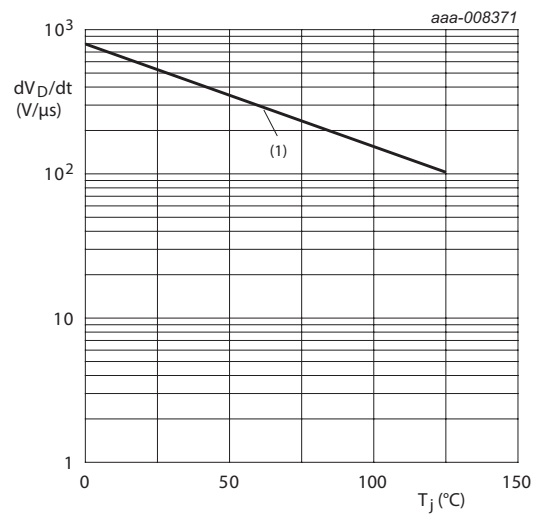


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



(1)  $R_{GK} = 100 \ \Omega$   
 Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

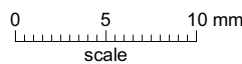
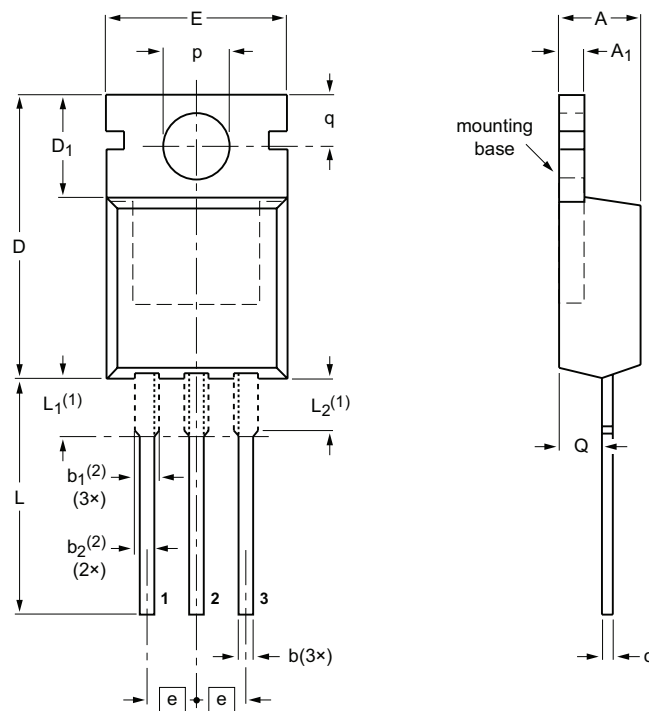


### 11. Package outline

Assembly factory: d & A

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78



**DIMENSIONS** (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b	b <sub>1</sub> (2)	b <sub>2</sub> (2)	c	D	D <sub>1</sub>	E	e	L	L <sub>1</sub> (1)	L <sub>2</sub> (1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

**Notes**

- 1. Lead shoulder designs may vary.
- 2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT78		3-lead TO-220AB	SC-46		08-04-23 08-06-13

## 12. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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