

1. General description

Planar passivated AC Thyristor Triac power switch in a TO220F "full pack" plastic package with self-protective capabilities against low and high energy transients. This "series CTN" triac will commute the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High junction operating temperature capability ($T_{j(max)} = 150\text{ °C}$)
- High minimum I_{GT} for guaranteed immunity to gate noise
- Full cycle AC conduction
- Isolated mounting base package
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Triggering in three quadrants only
- Planar passivated for voltage ruggedness and reliability
- High commutation capability with maximum false trigger immunity
- Very high immunity to false turn-on by dV/dt and IEC 61000-4-4 fast transient
- Package meets UL94V0 flammability requirement
- Package is RoHS compliant
- Package meets UL1557 isolation test requirement rated at 2500V RMS

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls
- Applications subject to high temperature ($T_{j(max)} = 150\text{ °C}$)

4. Quick reference data

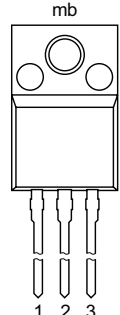
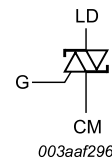
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 106\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	80	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	-	88	A
T_j	junction temperature		-	-	150	°C
V_{PP}	peak pulse voltage	$T_j = 25\text{ °C}$; non-repetitive, off-state; Fig. 6	-	-	2	kV

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; Fig. 8	5	-	35	mA
		V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; Fig. 8	5	-	35	mA
		V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; Fig. 8	5	-	35	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; Fig. 10	-	-	40	mA
V _T	on-state voltage	I _T = 10 A; T _j = 25 °C; Fig. 11	-	-	1.5	V
V _{CL}	clamping voltage	I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C	850	-	-	V
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	2000	-	-	V/μs
dI _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 8 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit	12	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common		
2	LD	load		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
ACTT8X-800CTN	TO220F	ACTT8X-800CTNQ	Tube	50	SOT186A	14-Nov-2013

7. Marking

Table 4. Marking codes

Type number	Marking codes	
	Assembly factory: d	Assembly factory: A
ACTT8X-800CTN	ACTT8X 800CTN PJdxxxx xx	ACTT8X 800CTN PJAxxxx xx

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 106\text{ }^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ }^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig 4 ; Fig 5	-	80	A
		full sine wave; $T_{j(init)} = 25\text{ }^\circ\text{C}$; $t_p = 16.7\text{ ms}$	-	88	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	32	A^2s
di_T/dt	rate of rise of on-state current	$I_G = 70\text{ mA}$	-	100	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
T_{stg}	storage temperature		-40	150	$^\circ\text{C}$
T_j	junction temperature		-	150	$^\circ\text{C}$
V_{pp}	peak pulse voltage	$T_j = 25\text{ }^\circ\text{C}$; non-repetitive, off-state; Fig 6	-	2	kV

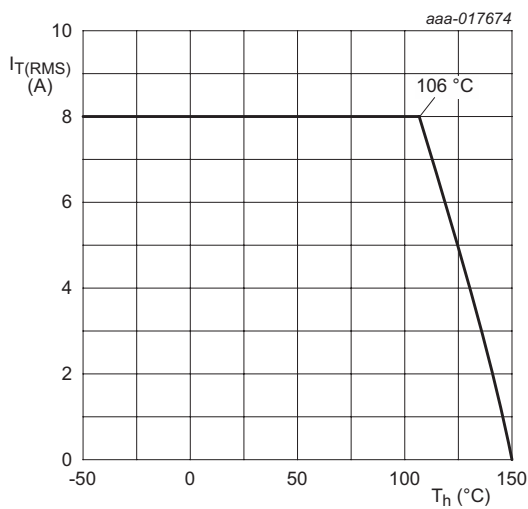


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

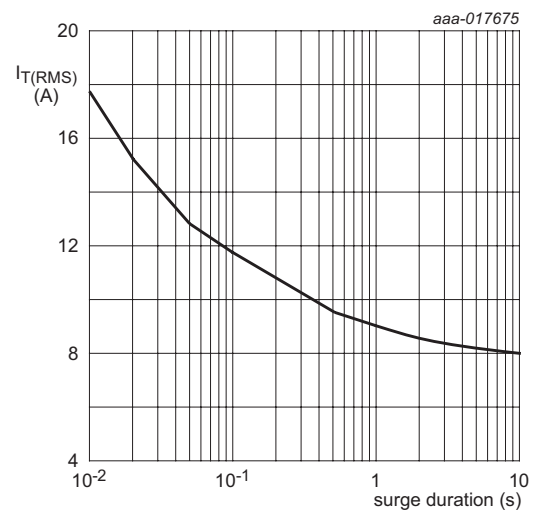


Fig. 2. RMS on-state current as a function of surge duration; maximum values
 $f = 50\text{ Hz}$; $T_h = 106\text{ }^\circ\text{C}$

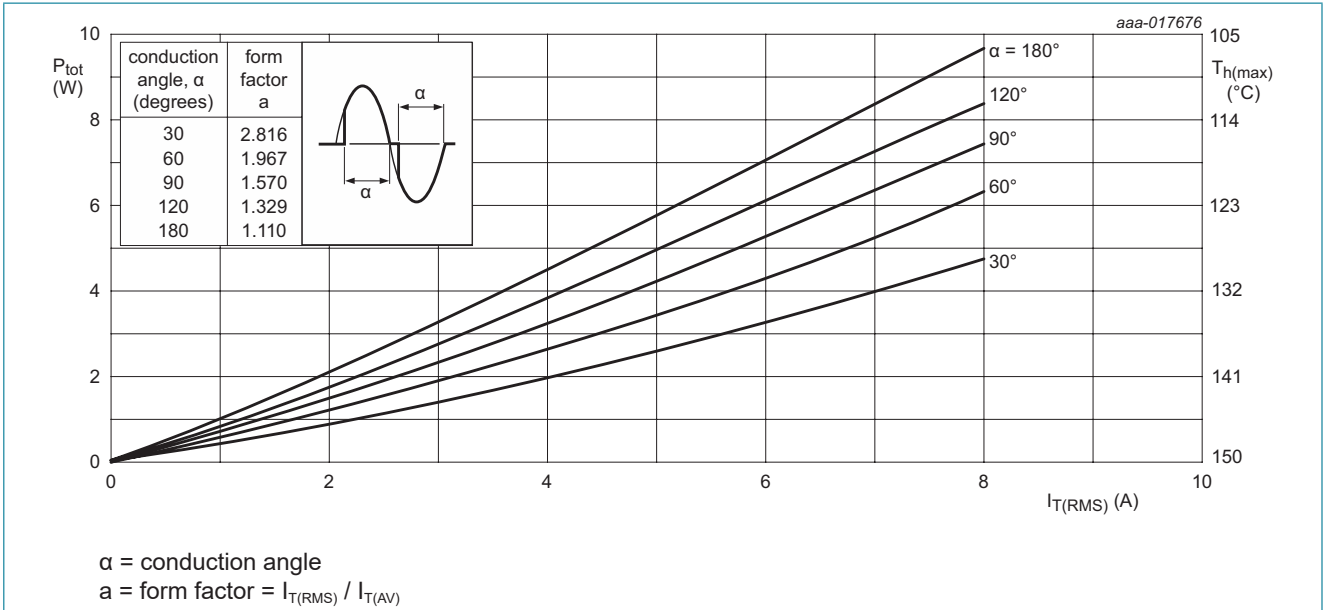


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

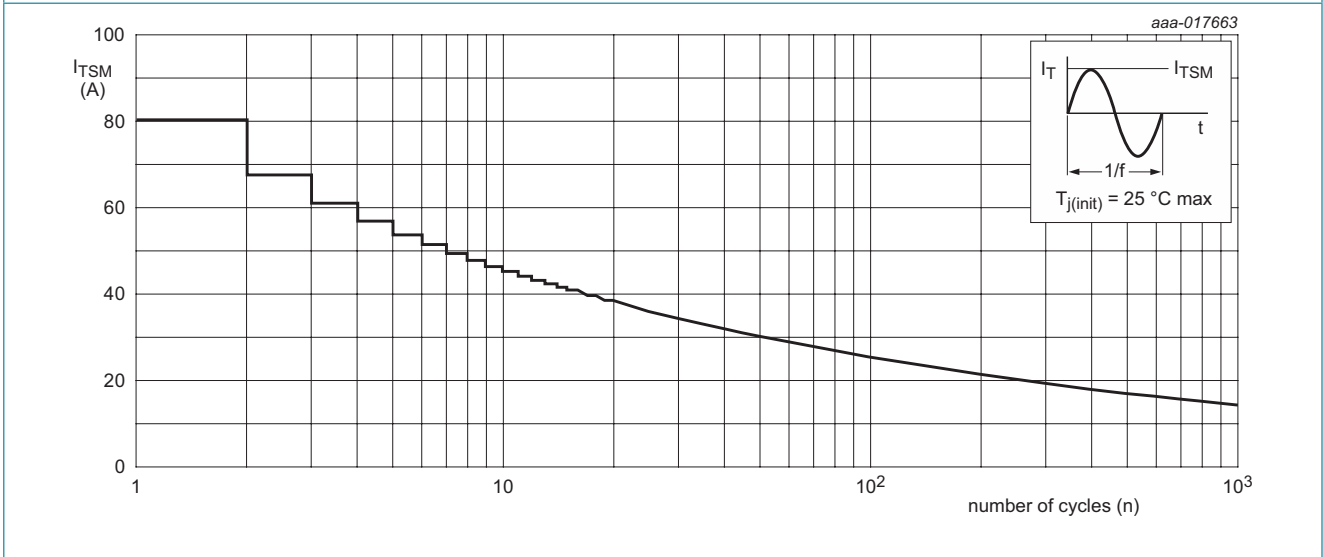


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

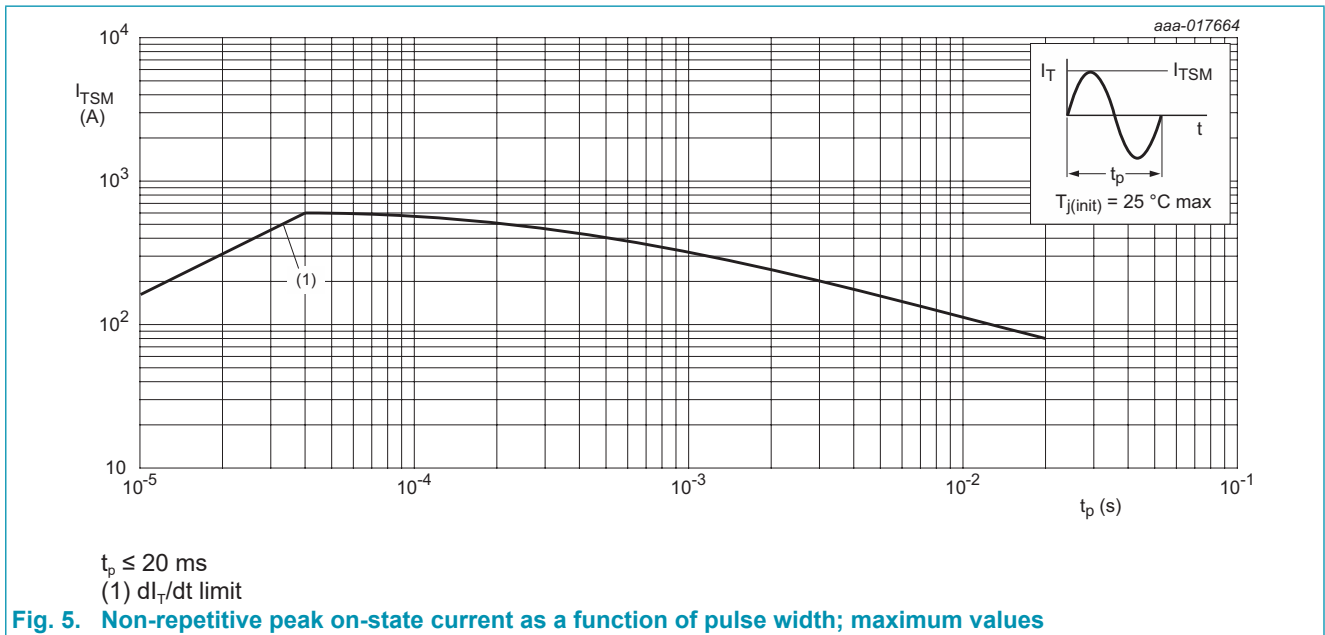


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

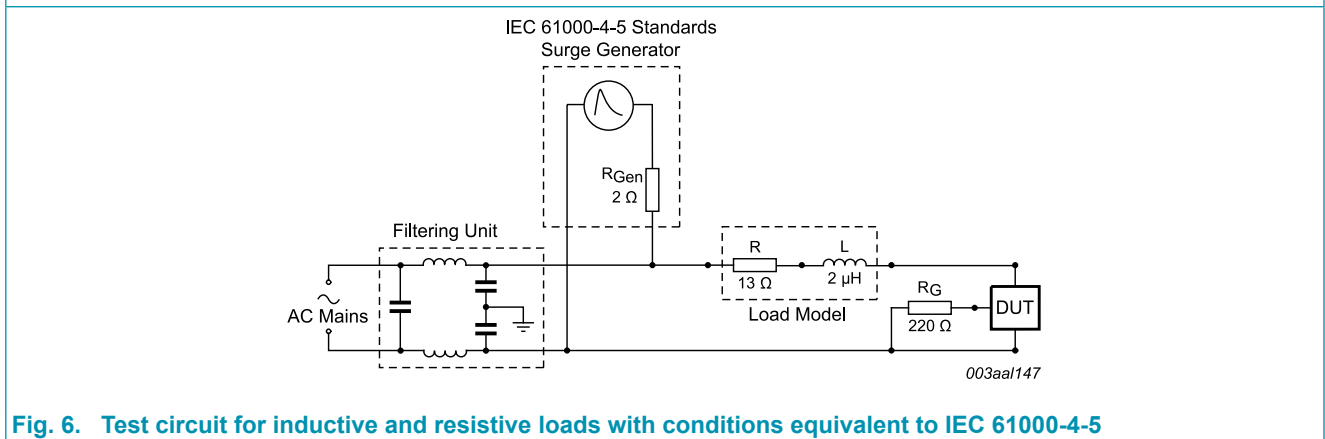


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full or half cycle; with heatsink compound Fig. 7	-	-	4.5	K/W
		full or half cycle; without heatsink compound	-	-	6.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W

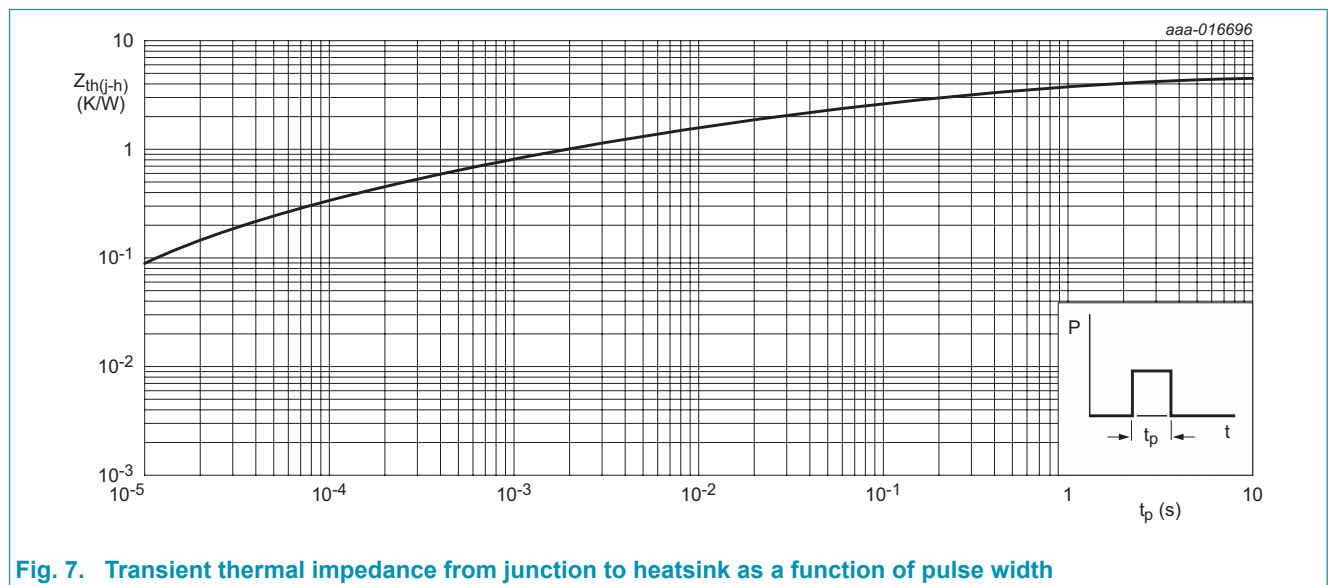


Fig. 7. Transient thermal impedance from junction to heatsink as a function of pulse width

10. Isolation characteristics

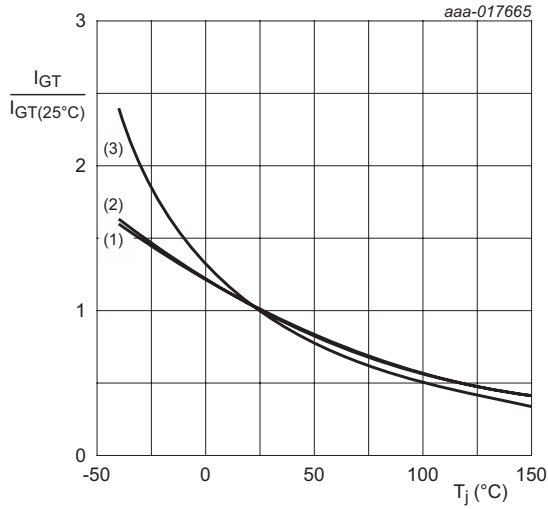
Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	sinusoidal waveform; from all pins to external heatsink; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_h = 25\text{ }^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from LD pin to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^\circ\text{C}$	-	10	-	pF

11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 100\text{ mA}; \text{LD+ G+}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 8}$	5	-	35	mA
		$V_D = 12\text{ V}; I_T = 100\text{ mA}; \text{LD+ G-}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 8}$	5	-	35	mA
		$V_D = 12\text{ V}; I_T = 100\text{ mA}; \text{LD- G-}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 8}$	5	-	35	mA
I_L	latching current	$V_D = 12\text{ V}; I_G = 100\text{ mA}; \text{LD+ G+}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 9}$	-	-	50	mA
		$V_D = 12\text{ V}; I_G = 100\text{ mA}; \text{LD+ G-}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 9}$	-	-	60	mA
		$V_D = 12\text{ V}; I_G = 100\text{ mA}; \text{LD- G-}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 9}$	-	-	50	mA
I_H	holding current	$V_D = 12\text{ V}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 10}$	-	-	40	mA
V_T	on-state voltage	$I_T = 10\text{ A}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 11}$	-	-	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 100\text{ mA}; T_J = 25\text{ }^\circ\text{C}; \text{Fig. 12}$	-	0.8	1	V
		$V_D = 400\text{ V}; I_T = 100\text{ mA}; T_J = 150\text{ }^\circ\text{C}$	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}; T_J = 25\text{ }^\circ\text{C}$	-	-	10	μA
		$V_D = 800\text{ V}; T_J = 150\text{ }^\circ\text{C}$	-	-	2	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}; t_p = 1\text{ ms}; T_J = 25\text{ }^\circ\text{C}$	850	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_J = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{exponential waveform}; \text{gate open circuit}$	4000	-	-	V/ μs
		$V_{DM} = 536\text{ V}; T_J = 150\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{exponential waveform}; \text{gate open circuit}$	2000	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_J = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 8\text{ A}; dV_{com}/dt = 20\text{ V}/\mu\text{s}; (\text{snubberless condition}); \text{gate open circuit}$	12	-	-	A/ms
		$V_D = 400\text{ V}; T_J = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 8\text{ A}; dV_{com}/dt = 10\text{ V}/\mu\text{s}; \text{gate open circuit}$	15	-	-	A/ms
		$V_D = 400\text{ V}; T_J = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 8\text{ A}; dV_{com}/dt = 1\text{ V}/\mu\text{s}; \text{gate open circuit}$	20	-	-	A/ms



- (1) LD+ G+
- (2) LD+ G-
- (3) LD- G-

Fig. 8. Normalized gate trigger current as a function of junction temperature

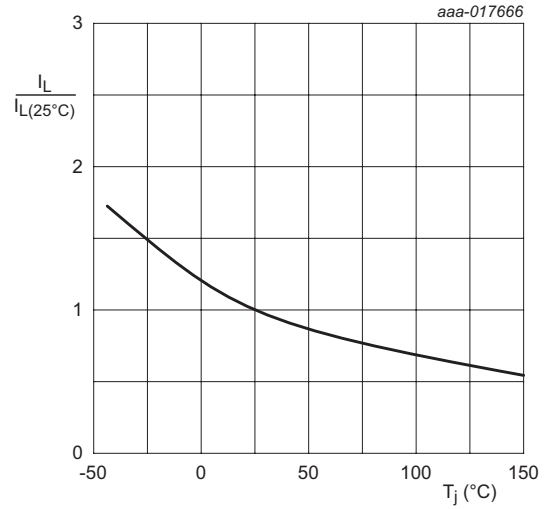


Fig. 9. Normalized latching current as a function of junction temperature

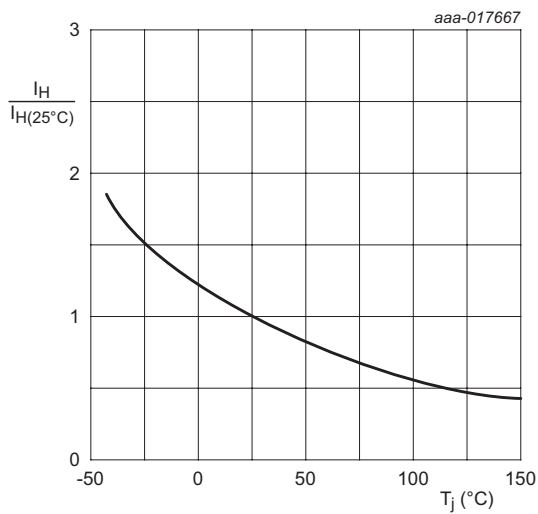
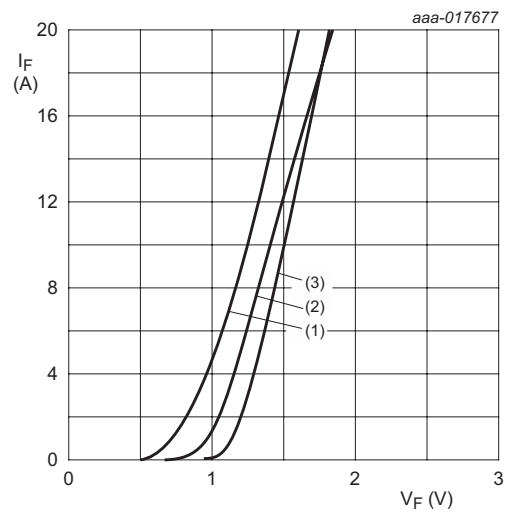


Fig. 10. Normalized holding current as a function of junction temperature



- $V_o = 1.123 \text{ V}; R_s = 0.025 \Omega$
- (1) $T_j = 150 \text{ }^\circ\text{C}$; typical values
 - (2) $T_j = 150 \text{ }^\circ\text{C}$; maximum values
 - (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 11. On-state current as a function of on-state voltage

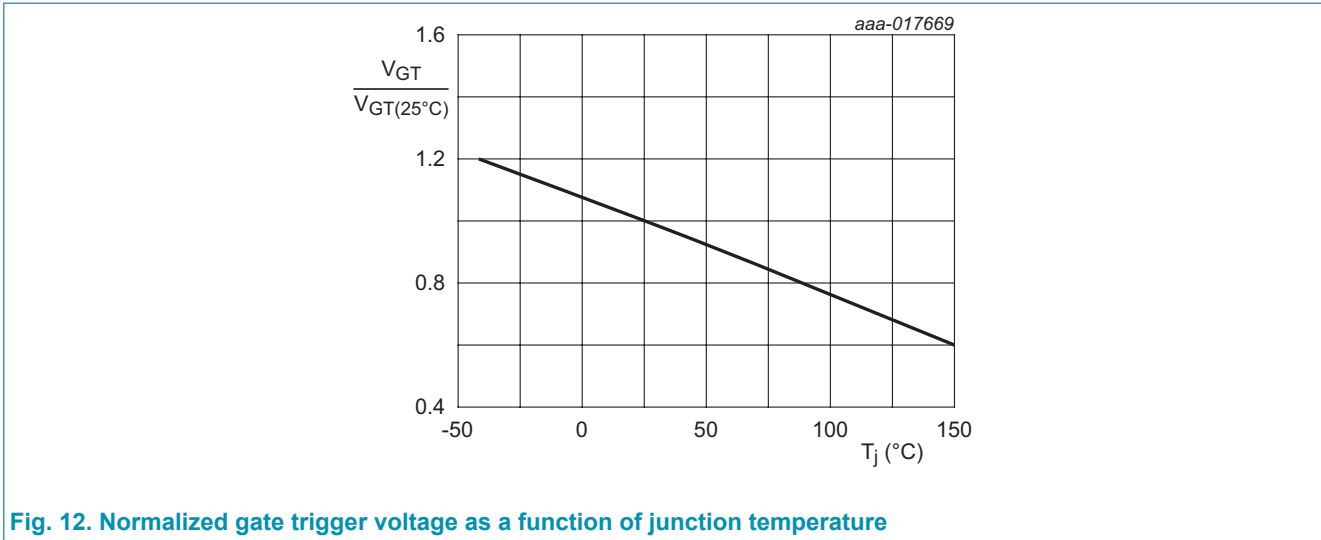


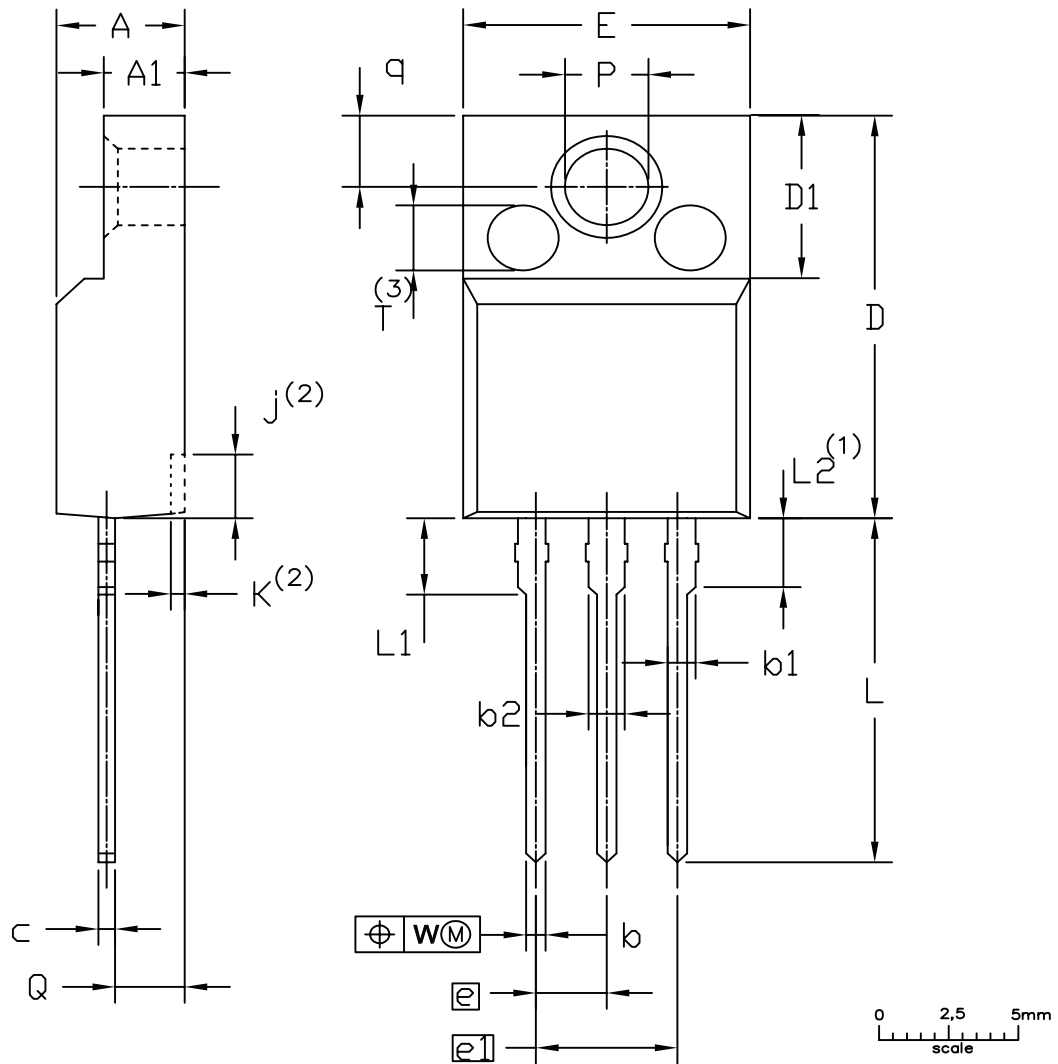
Fig. 12. Normalized gate trigger voltage as a function of junction temperature

12. Package outline

Assembly factory: d & A

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"

SOT186A



UNIT	A	A ₁	b	b ₁	b ₂	c	D	D ₁	E	e	e ₁	j ⁽²⁾	k ⁽²⁾	L	L ₁	L ₂ ⁽¹⁾ max.	P	Q	q	W	T ⁽³⁾
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes

1. Terminal dimensions within this zone are uncontrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT186A		3 LEADS TO220F			2013-11-14

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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