

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) module in WeEnTOP-B for use in applications requiring high blocking voltage capability, high inrush current capability and high thermal cycling performance.

2. Features and benefits

- Planar passivated thyristor chips for voltage ruggedness and reliability
- Top-side cooling
- Compact design
- One screw mounting
- Heat transfer and isolation through direct copper bonded aluminum oxide ceramic (DBC)
- Package is RoHS compliant

3. Applications

- Soft starters
- UPS
- Temperature control
- Lighting control
- AC power control

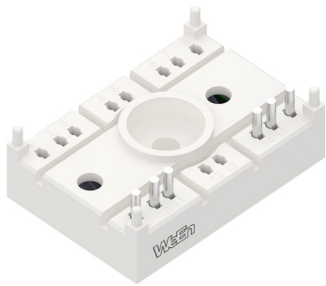
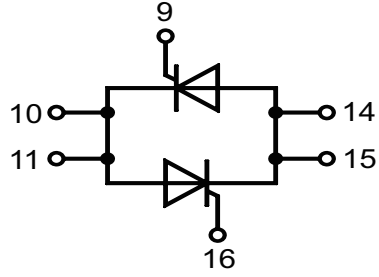
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values			Unit
Absolute maximum rating							
V_{DRM}	repetitive peak forward voltage			1200			V
V_{RRM}	repetitive peak reverse voltage			1200			V
$I_{T(RMS)}$	RMS on-state current	half sine wave		134			A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 10\text{ ms}$		2000			A
		half sine wave; $T_{j(\text{init})} = 125\text{ °C}$; $t_p = 10\text{ ms}$		1800			A
		half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$		2200			A
		half sine wave; $T_{j(\text{init})} = 125\text{ °C}$; $t_p = 8.3\text{ ms}$		1870			A
Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$		30	-	100	mA
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$		-	-	1.50	V
V_T	on-state voltage	$I_T = 240\text{ A}$; $T_j = 25\text{ °C}$		-	-	1.70	V

5. Pinning information

Table 2. Pinning information

Simplified outline	Graphic symbol
	

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
WAT120TBS12	WeEnTOP-B	WAT120TBS12T	EPE	30	WeEnTOP-BPAT-A	05-Nov-2024

7. Marking

Table 4. Marking codes

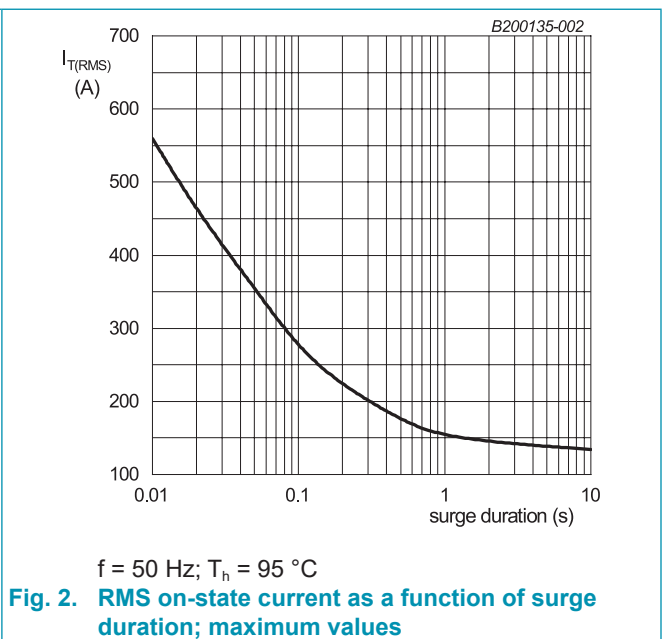
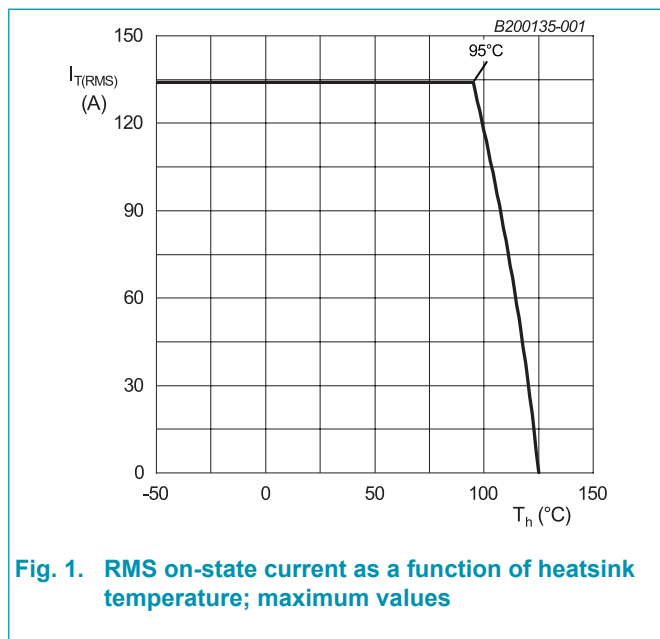
Type number	Marking codes
WAT120TBS12	WAT120TBS12

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Values	Unit
V_{DRM}	repetitive peak forward voltage			1200	V
V_{RRM}	repetitive peak reverse voltage			1200	V
$I_{T(RMS)}$	RMS on-state current	half sine wave		134	A
I_{TSM}	non-repetitive peak onstate current	half sine wave; $T_{j(Init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$		2000	A
		half sine wave; $T_{j(Init)} = 125\text{ °C}$; $t_p = 10\text{ ms}$		1800	A
		half sine wave; $T_{j(Init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$		2200	A
		half sine wave; $T_{j(Init)} = 125\text{ °C}$; $t_p = 8.3\text{ ms}$		1870	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse		20	kA^2s
di_T/dt	rate of rise of on-state current	$I_G = 200\text{ mA}$; $T_j = 125\text{ °C}$		200	$A/\mu s$
I_{GM}	peak gate current			10	A
V_{RGM}	peak reverse gate voltage			5	V
P_{GM}	peak gate power			20	W
$P_{G(AV)}$	average gate power	over any 20 ms period		0.5	W
T_{vj}	virtual junction temperature			-40 to 125	$^{\circ}C$
T_{op}	operation temperature			-40 to 125	$^{\circ}C$
T_{stg}	storage temperature			-40 to 125	$^{\circ}C$



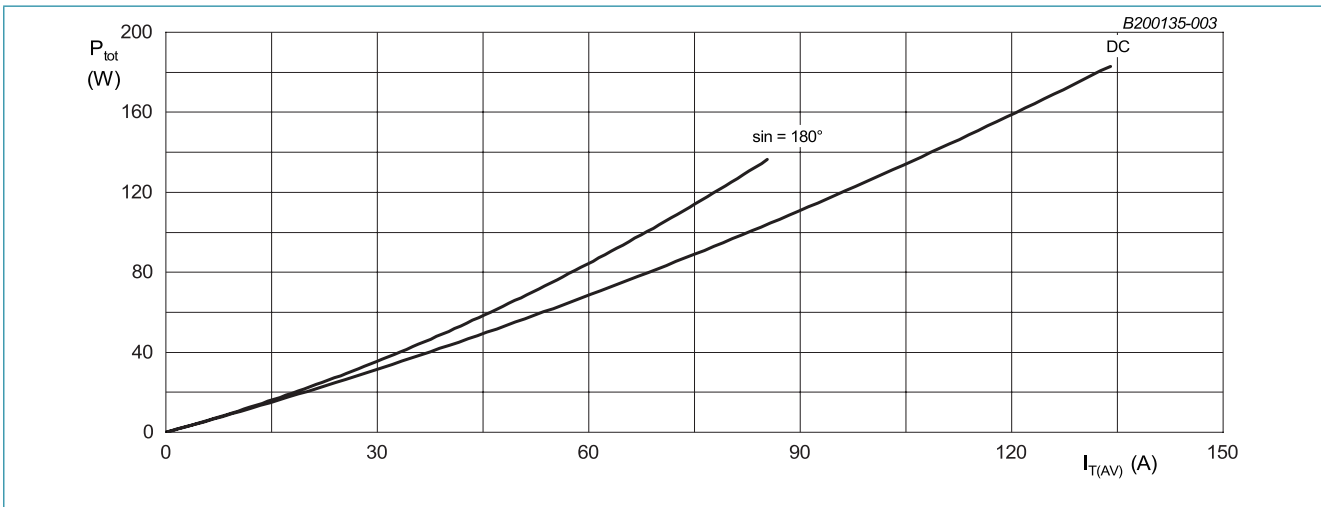


Fig. 3. Total power dissipation as a function of average on-state current; maximum values

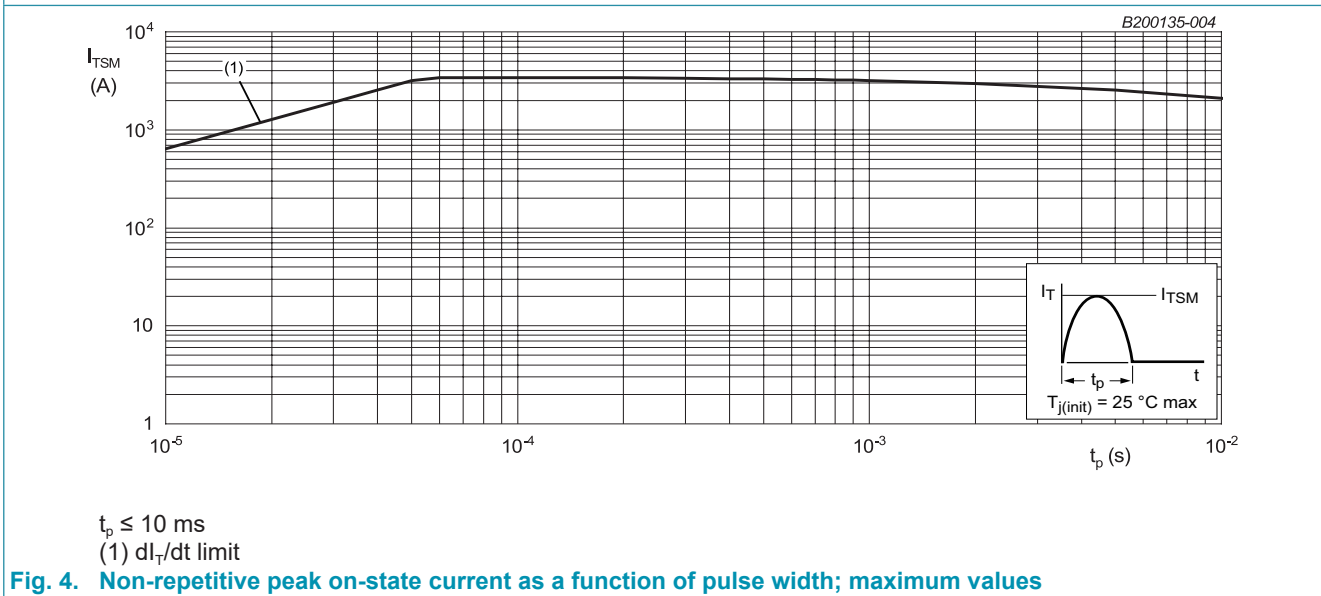


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	per thyristor		-	-	0.44	K/W
		per module		-	-	0.22	K/W

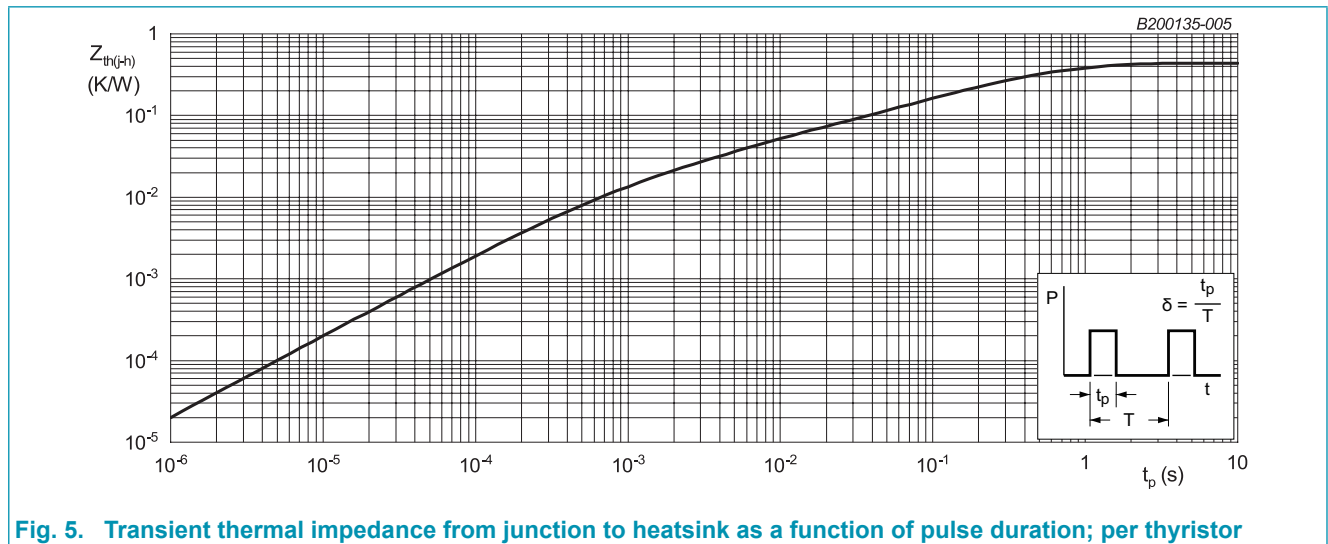


Fig. 5. Transient thermal impedance from junction to heatsink as a function of pulse duration; per thyristor

10. Package characteristics

Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
V_{isol}	isolation voltage	50/60 Hz; RMS; $I_{ISOL} \leq 1$ mA; $t = 1$ second; AC		-	-	3600	V
		50/60 Hz; RMS; $I_{ISOL} \leq 1$ mA; $t = 1$ minute; AC		-	-	2500	V

11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$		30	-	100	mA
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$		-	-	1.50	V
		$V_D = 2/3 V_{DRM}; I_T = 0.1\text{ A}; T_j = 125\text{ }^\circ\text{C}$		0.25	-	-	V
I_{GD}	gate non-trigger current	$T_j = 125\text{ }^\circ\text{C}$		-	-	8.5	mA
V_{GD}	gate non-trigger voltage	$T_j = 125\text{ }^\circ\text{C}$		-	-	0.2	V
I_L	latching current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C}$		-	-	300	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C}$		-	-	200	mA
V_T	on-state voltage	$I_T = 240\text{ A}; T_j = 25\text{ }^\circ\text{C}$		-	-	1.70	V
V_{TO}	threshold voltage	$T_j = 125\text{ }^\circ\text{C}$		-	-	0.96	V
r_T	slope resistance	$T_j = 125\text{ }^\circ\text{C}$		-	-	3	m Ω
I_D	off-state current	$V_D = 1200\text{ V}; T_j = 25\text{ }^\circ\text{C}$		-	-	100	μA
		$V_D = 1200\text{ V}; T_j = 125\text{ }^\circ\text{C}$		-	-	15	mA
I_R	reverse current	$V_R = 1200\text{ V}; T_j = 25\text{ }^\circ\text{C}$		-	-	100	μA
		$V_R = 1200\text{ V}; T_j = 125\text{ }^\circ\text{C}$		-	-	15	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 804\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\% \text{ of } V_{DRM}); \text{exponential waveform}; \text{gate open circuit}$		1500	-	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 40\text{ A}; V_D = 800\text{ V}; I_G = 100\text{ mA}; (dI_G/dt)_M = 1\text{ A}/\mu\text{s}; T_j = 25\text{ }^\circ\text{C}$		-	2	-	μs
t_q	commutated turn-off time	$I_{TM} = 2\text{ A}; t_p = 50\text{ } \mu\text{s}; dV/dt = 5\text{ V}/\mu\text{s}; dI/dt = 30\text{ A}/\mu\text{s}; T_j = 25\text{ }^\circ\text{C}$		-	150	-	μs

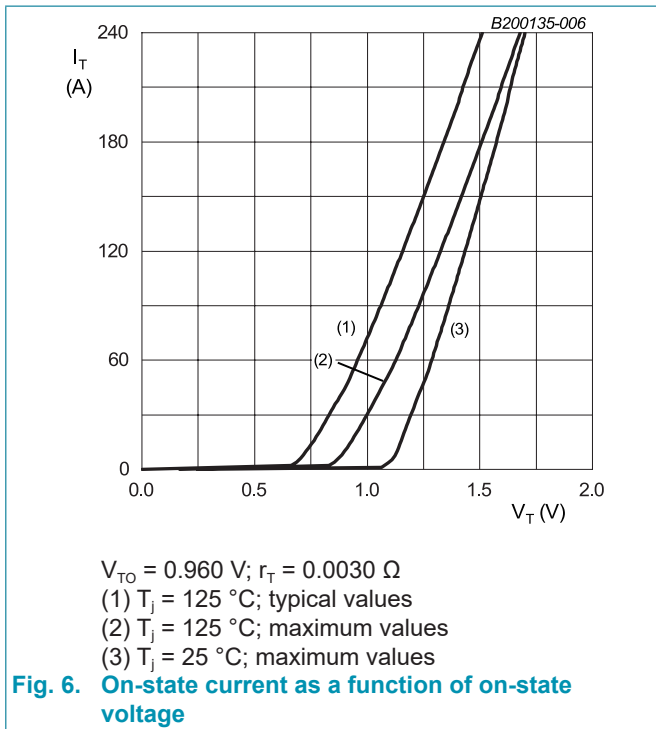


Fig. 6. On-state current as a function of on-state voltage

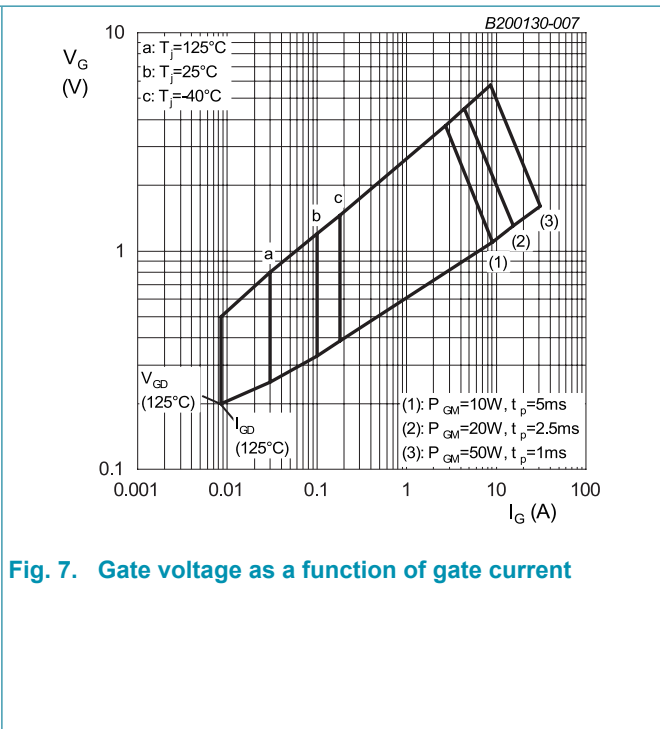
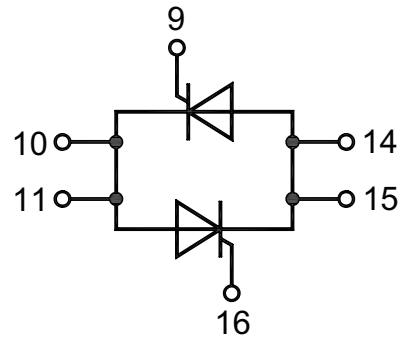
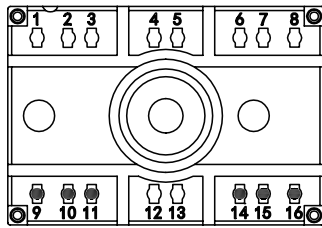


Fig. 7. Gate voltage as a function of gate current

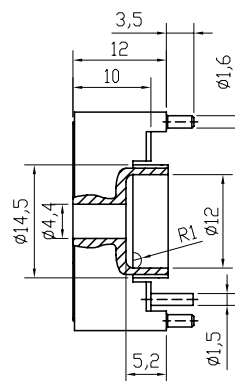
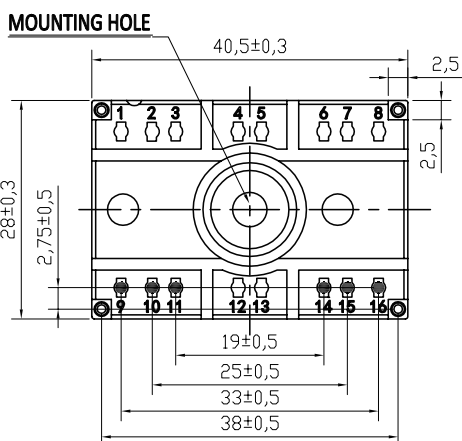
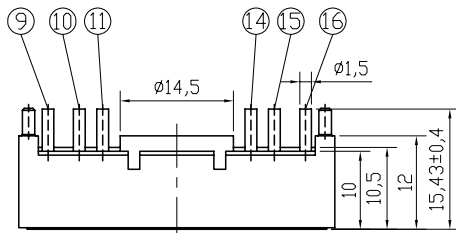
12. Package outline

Dimensions in mm

Pinout



Package Outline



Suggested hole diameter in the PCB for solder pins and mounting pins: 2mm

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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