BTA302W-800ET

3Q Hi-Com Triac

Rev.01 - 13 January 2025 Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT223 surface mountable plastic package. This "series ET" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers.

2. Features and benefits

- 3Q technology for improved noise immunity
- Direct triggering from low power drivers and logic ICs
- High commutation capability with sensitive gate
- High immunity to false turn-on by dV/dt
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

3. Applications

- General purpose motor control
- Small loads in washing machines
- Solenoid drivers

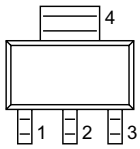
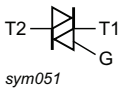
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Notes	Values			Unit
Absolute maximum rating							
V_{DRM}	repetitive peak off-state voltage			800			V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 115$ °C; Fig. 1; Fig. 2; Fig. 3		2			A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		17			A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		18.7			A
T_j	operating junction temperature			-40 to 150			°C
Symbol	**Parameter**	**Conditions**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 0.1$ A; T2+ G+; $T_j = 25$ °C; Fig. 9		1	-	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2+ G-; $T_j = 25$ °C; Fig. 9		1	-	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2- G-; $T_j = 25$ °C; Fig. 9		1	-	10	mA
I_H	holding current	$V_D = 12$ V; $T_j = 25$ °C; Fig. 11		-	-	12	mA
V_T	on-state voltage	$I_T = 2.0$ A; $T_j = 25$ °C; Fig. 12		-	1.35	1.55	V

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
4	T2	main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BTA302W-800ET	SOT223	BTA302W-800ETF	Reel	4000	SOT223	16-Mar-2006

7. Marking

Table 4. Marking codes

Type number	Marking codes	
	Assembly factory: d	Assembly factory: L
BTA302W-800ET	Jdxxx 302W8E	JLxxx 302W8E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Notes	Max	Unit
V_{DRM}	repetitive peak off-state voltage			800	V
V_{RRM}	repetitive peak reverse voltage			800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{sp} \leq 115$ °C; Fig 1; Fig 2; Fig 3		2	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig 4; Fig 5		17	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		18.7	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		1.4	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 20$ mA		100	A/µs
I_{GM}	peak gate current			2	A
P_{GM}	peak gate power			5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		0.1	W
T_{stg}	storage temperature			-40 to 150	°C
T_j	operating junction temperature			-40 to 150	°C

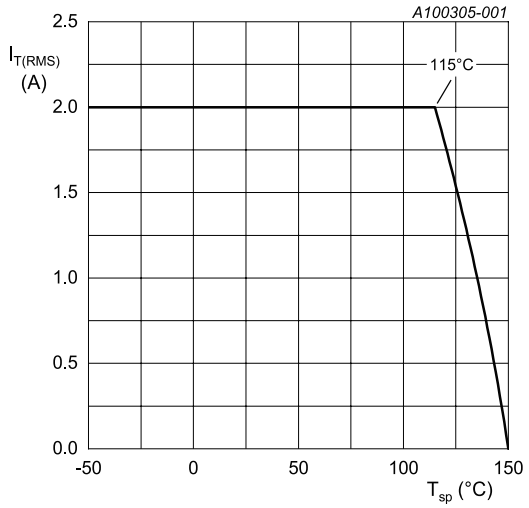
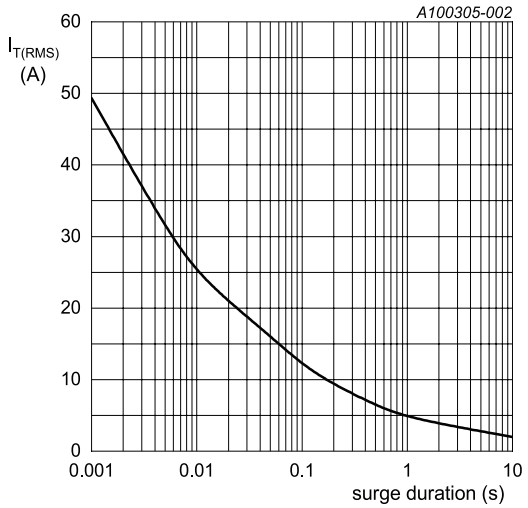
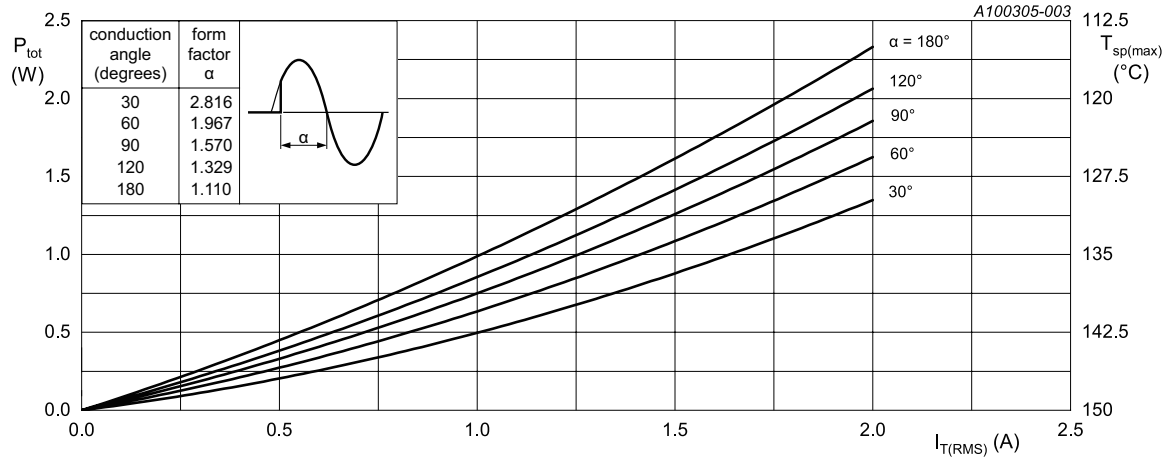


Fig. 1. RMS on-state current as a function of solder point temperature; maximum values



f = 50 Hz; T_{sp} = 115 °C

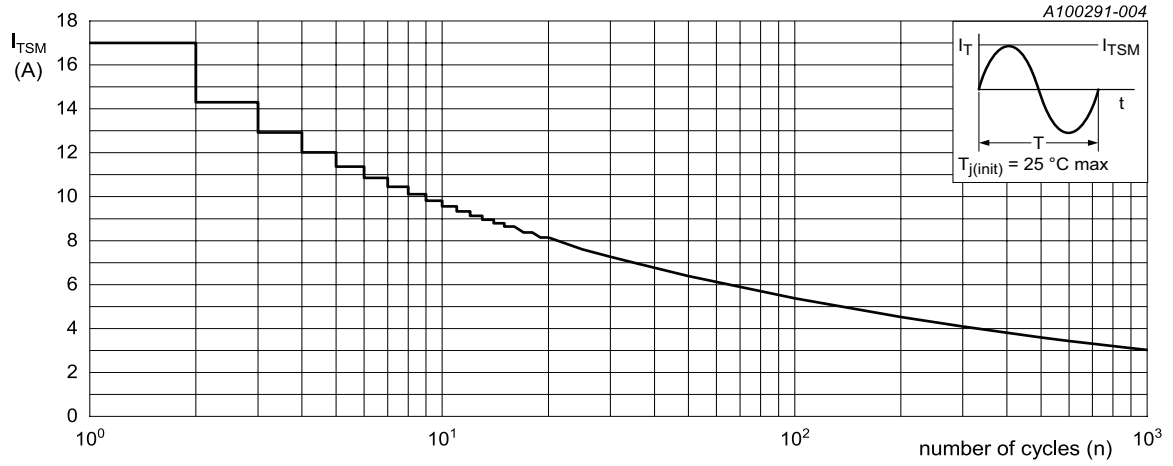
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

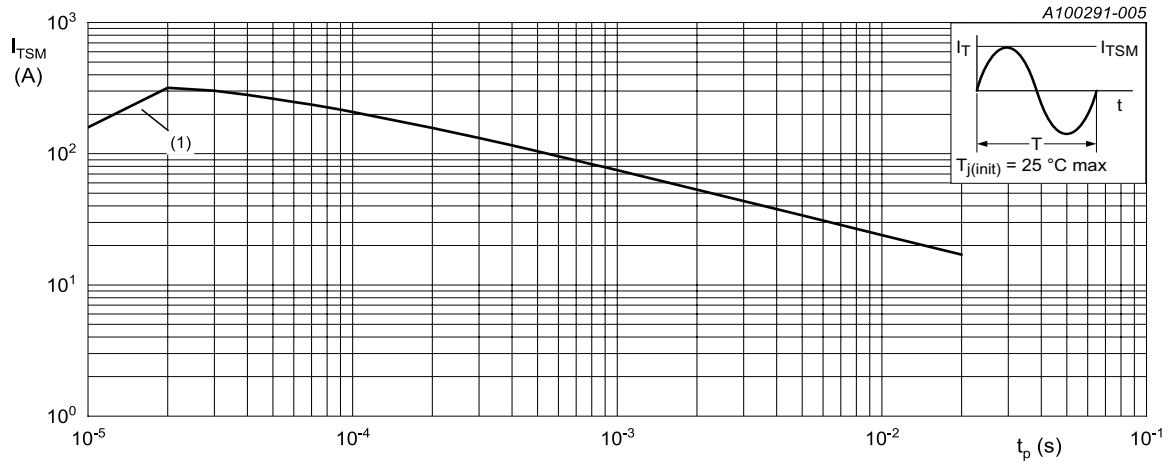
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full cycle; Fig 6		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; printed-circuit board mounted; minimum footprint; Fig 7		-	156	-	K/W
		in free air; printed-circuit board mounted; pad area; Fig 8		-	70	-	K/W

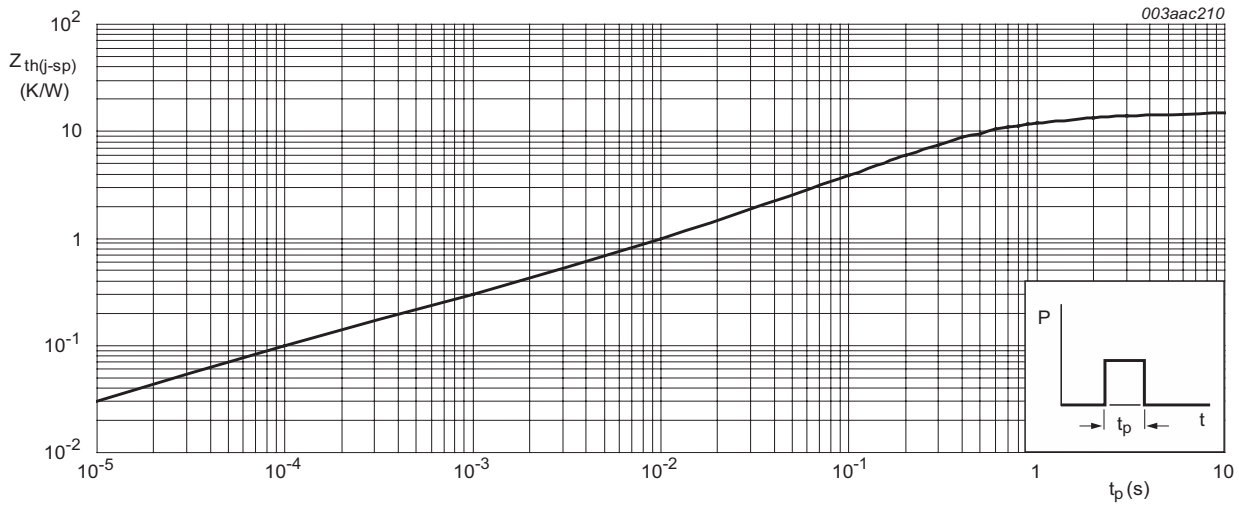
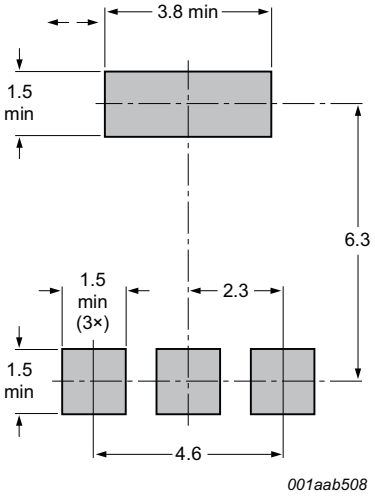
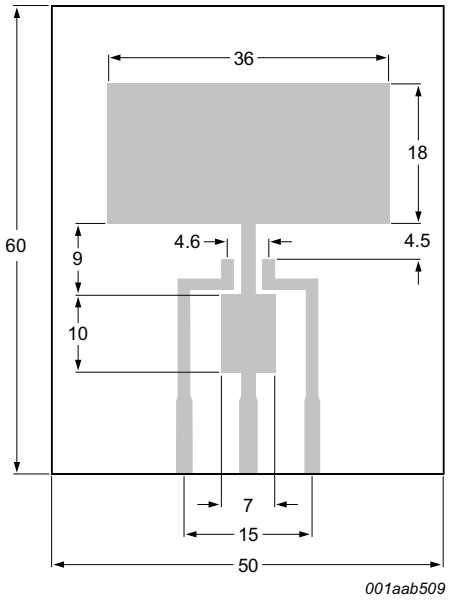


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width



All dimensions are in mm

Fig. 7. Minimum footprint SOT223



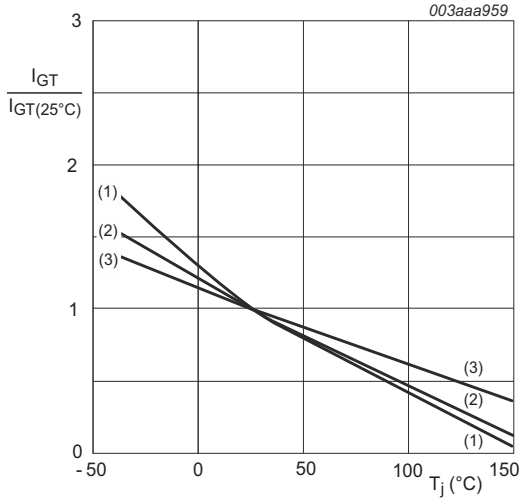
All dimensions are in mm
Printed circuit board:
FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 8. Printed circuit board pad area: SOT223

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Notes	Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 9		1	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 9		1	-	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 9		1	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 10		-	-	12	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 10		-	-	20	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 10		-	-	12	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 11		-	-	12	mA
V_T	on-state voltage	I_T = 2.0 A; T_j = 25 °C; Fig. 12		-	1.35	1.55	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 13		-	0.7	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C		0.2	0.3	-	V
I_D	off-state current	V_D = 800 V; T_j = 150 °C		-	-	2	mA
I_R	reverse current	V_R = 800 V; T_j = 150 °C		-	-	2	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		600	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 1.0 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit		2.5	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 1.0 A; dV_{com}/dt = 10 V/µs; (snubberless condition); gate open circuit		3.5	-	-	A/ms



(1) T2- G-
(2) T2+ G-
(3) T2+ G+

Fig. 9. Normalized gate trigger current as a function of junction temperature

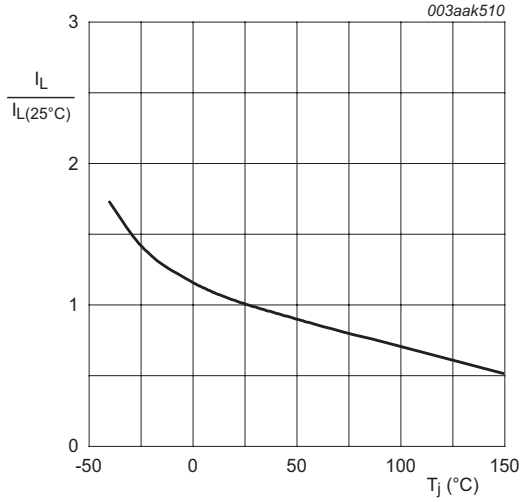


Fig. 10. Normalized latching current as a function of junction temperature

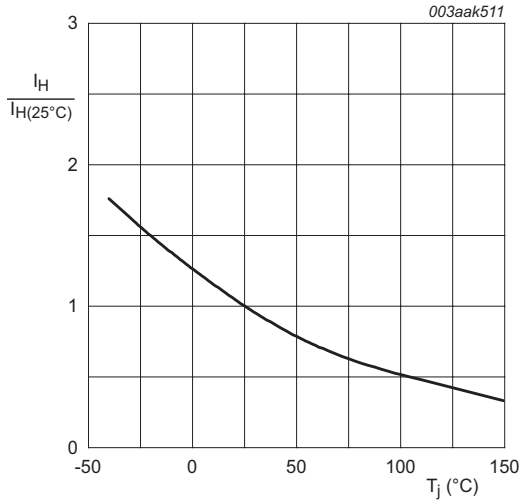
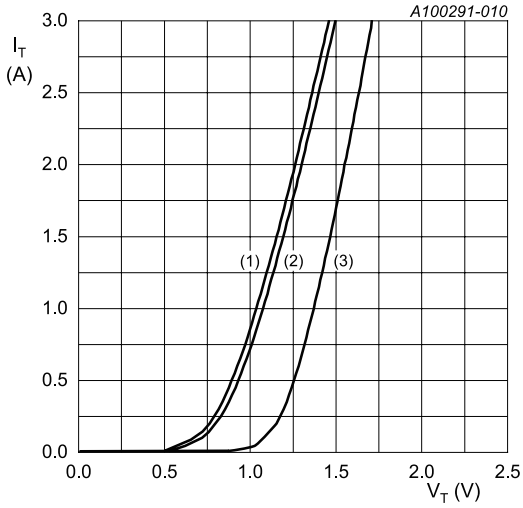


Fig. 11. Normalized holding current as a function of junction temperature



V_o = 0.900 V; R_s = 0.1775 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 12. On-state current as a function of on-state voltage

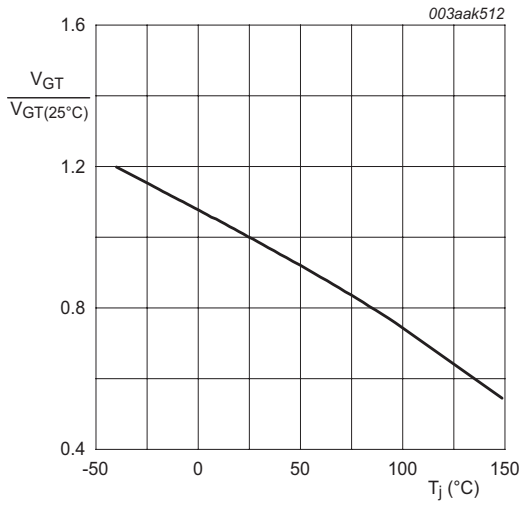
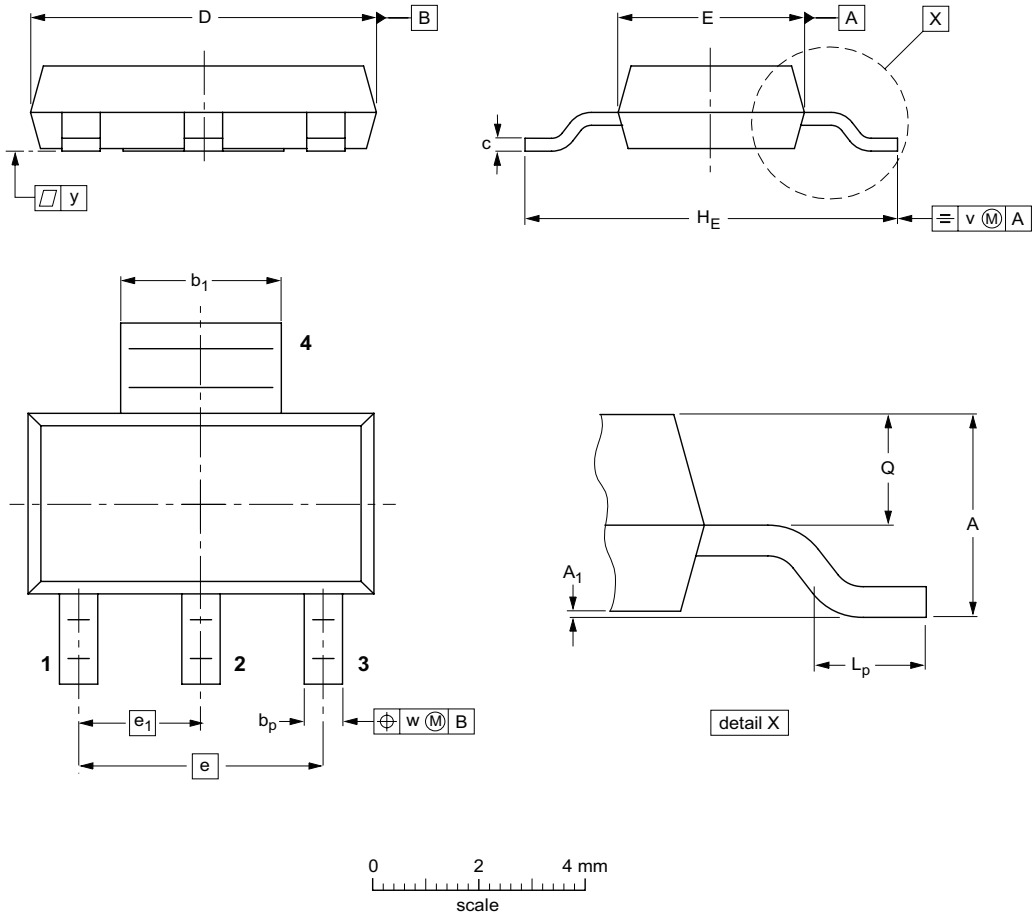


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

1. General description 1
2. Features and benefits 1
3. Applications 1
4. Quick reference data 1
5. Pinning information 2
6. Ordering information 2
7. Marking 2
8. Limiting values 3
9. Thermal characteristics 5
10. Characteristics 7
11. Package outline 10
12. Legal information 11
13. Contents 13

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